XT25BF256B

Quad IO Serial NOR Flash
Datasheet

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Serial NOR Flash Memory

3.3V Multi I/O with 4KB, 32KB & 64KB Sector/Block Erase

- **256M -bit Serial Flash**
  - 32,768K-bytes
  - 256 bytes per programmable page
- **Standard, Dual, Quad SPI, DTR**
  - Standard SPI: SCLK, CS#, SI, SO
  - Dual SPI: SCLK, CS#, IO0, IO1
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - QPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - SPI/QPI DTR (Double Transfer Rate) Read
- **Flexible Architecture**
  - Sector of 4K-bytes
  - Block of 32/64k-bytes
- **Advanced security Features**
  - 2*1024-Bytes Security Registers With OTP Lock
- **Support 128 bits Unique ID**
- **Software Write Protection**
  - Write protect all/portion of memory via software
  - Top or Bottom, Sector or Block selection
  - Advanced Sector Protection
- **3 or 4-Byte Addressing Mode**
- **Continuous Read With 8/16/32/64-byte Wrap**
- **Erase/Program Suspend/Resume**
- **Package Options**
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- **Temperature Range & Moisture Sensitivity Level**
  - Industrial Level Temperature. (-40°C to +85°C), MSL3
- **Power Consumption**
  - 6mA typical active read current
  - 0.5uA typical Deep Power-Down current
- **Single Power Supply Voltage**
  - 2.70~3.60V
- **Endurance and Data Retention**
  - Typical 100,000 Program/Erase Cycle
  - 20-year Data Retention typical
- **High Speed Clock Frequency**
  - 120MHz for fast read with 30pF load
  - Dual I/O Data transfer up to 208Mbit/s
  - Quad I/O Data transfer up to 416Mbit/s
  - QPI Mode Data transfer up to 320Mbit/s
  - DTR Quad I/O Data transfer up to 400Mbit/s
- **Program/Erase Speed**
  - Page Program time: 0.25ms typical
  - Sector Erase time: 40ms typical
  - Block Erase time: 0.15/0.22s typical
  - Chip Erase time: 70s typical

CONTENTS

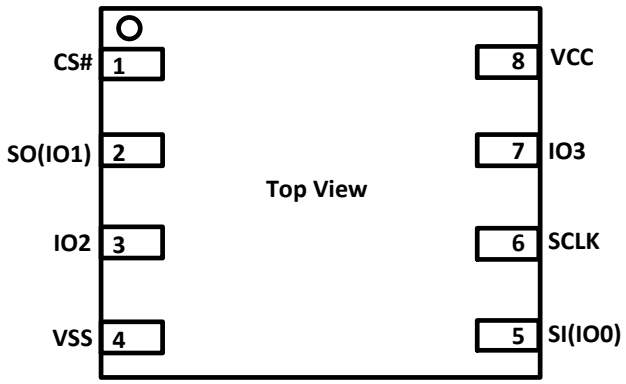
1. GENERAL DESCRIPTION

The XT25BF256B (256M-bit) Serial flash supports standard Serial Peripheral Interface (SPI), Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2, and I/O3.

1.1. Available Ordering OPN

OPN	Package Type	Package Carrier
XT25BF256BWSIGT	WSON8 8x6mm	Tape & Reel

1.2. Connection Diagram



8-PIN WSON

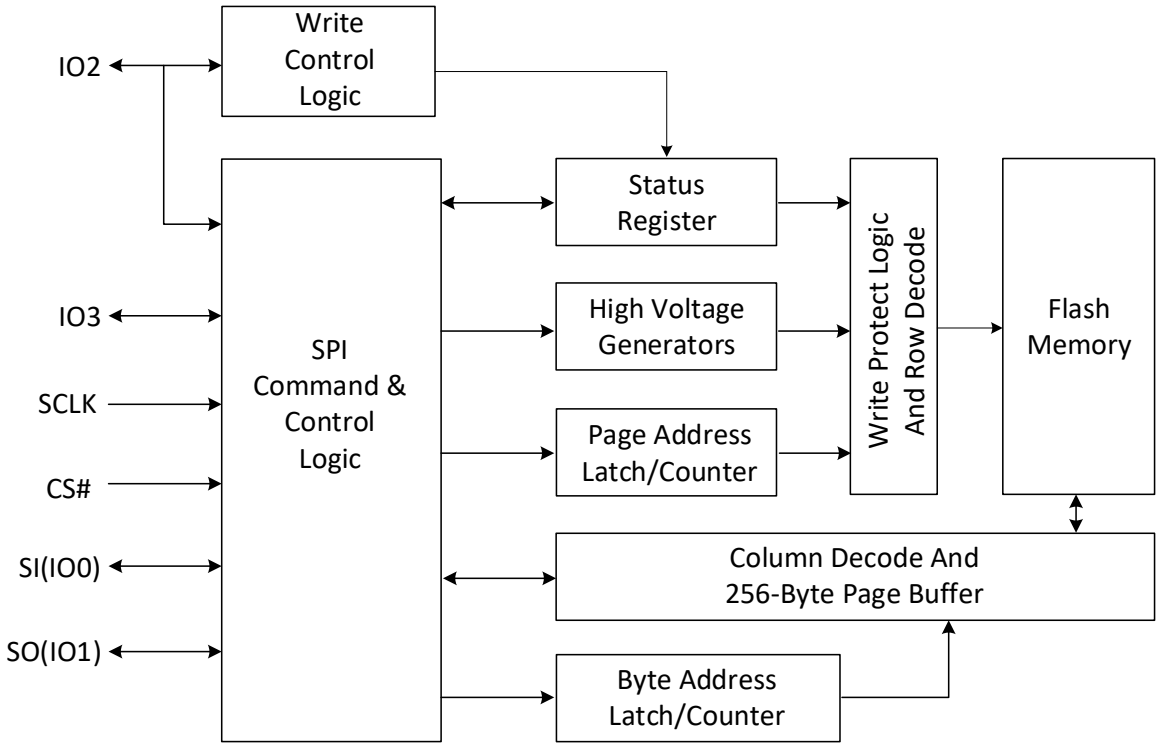
1.3. Pin Description

WSON8

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	IO2	I/O	Data Input Output 2
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	IO3	I/O	Data Input Output 3
8	VCC		Power Supply

Note:
1. IO0-IO3 are used for Quad SPI instructions.

1.4. Block Diagram



1.5. Memory Description

Uniform Block Sector Architecture

Block(64K-byte)	Block(32K-byte)	Sector(4K-byte)	Address Range	
511	1023	8191	1FFF000H	1FFFFFFH
		……	……	……
		8184	1FF8000H	1FF8FFFH
	1022	8183	1FF7000H	1FF7FFFH
		……	……	……
		8176	1FF0000H	1FF0FFFH
510	1021	8175	1FEF000H	1FEFFFFH
		……	……	……
		8168	1FE8000H	1FE8FFFH
	1020	8167	1FE7000H	1FE7FFFH
		……	……	……
		8160	1FE0000H	1FE0FFFH
……		……	……	……
		……	……	……
		……	……	……
1	3	31	01F000H	01FFFFH
		……	……	……
		24	018000H	018FFFH
	2	23	017000H	017FFFH
		……	……	……
		16	010000H	010FFFH
0	1	15	00F000H	00FFFFH
		……	……	……
		8	008000H	008FFFH
	0	7	007000H	007FFFH
		……	……	……
		0	000000H	000FFFH

2. DEVICE OPERATION

2.1. SPI Mode

Standard SPI

The device features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The device supports Dual SPI operation when using the "Dual Output Fast Read", "Dual I/O Fast Read" and "DTR Fast Read Dual I/O" (3BH, 3CH, BBH, BCH and BDH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The device supports Quad SPI operation when using the "Quad Output Fast Read", "Quad I/O Fast Read", "Quad I/O Word Fast Read" and "DTR Fast Read Quad I/O" (6BH, 6CH, EBH, ECH, E7H, EDH, EEH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, IO2 and IO3.

2.2. QPI Mode

The device supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the "Enable the QPI (38H)" command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. "Enable the QPI (38H)" and "Disable the QPI (FFH)" commands are used to switch between these two modes. Upon power-up and after software reset using "Enable Chip Reset (66H)" and "Reset (99H)" command, the default state of the device is Standard/Dual/Quad SPI mode.

2.3. DTR Read

To effectively improve the read operation throughput without increasing the serial clock frequency, The device introduces multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

2.4. The Reset Signaling Protocol (JEDEC 252)

The protocol consists of two phases: reset request, and completion (a device internal reset).

Reset Request

1. CS# is driven active low to select the device Note1
2. Clock (SCLK) remains stable in either a high or low state Note 2
3. SI / IO0 is driven low by the bus master, simultaneously with CS# going active low Note 3
4. CS# is driven inactive Note 4

Repeat the steps 1-4 each time alternating the state of SI Note 5

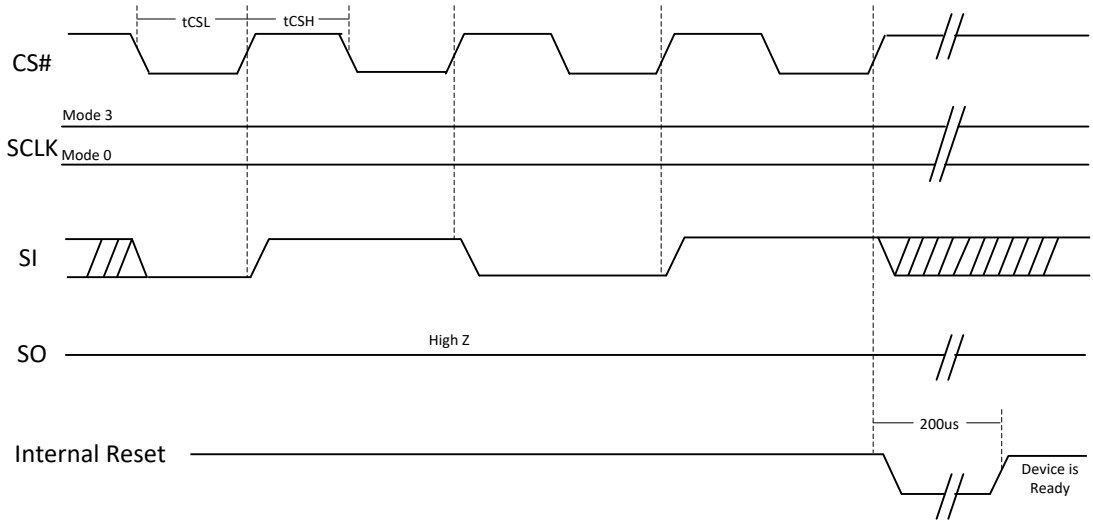
NOTE 1 This powers up the device.
NOTE 2 This prevents any confusion with a command, as no command bits are transferred (clocked).
NOTE 3 No SPI bus slave drives SI during CS# low before a transition of SCLK, i.e., slave streaming output active is not allowed until after the first edge of SCLK.
NOTE 4 The slave captures the state of SI on the rising edge of CS#.
NOTE 5 SI is low on the first CS#, high on the second, low on the third, high on the fourth (This provides a 5h pattern, to differentiate it from random noise).

Reset Completion

After the fourth CS# pulse, the slave triggers its internal reset.

Timing Diagram and Timing Parameters

Reset Signaling Protocol



3. STATUS REGISTER

Status Register-1

S7	S6	S5	S4	S3	S2	S1	S0
Reserved	T/B	BP3	BP2	BP1	BP0	WEL	WIP
Reserved	Top/Bottom Protect Bit	Block Protect Bit	Block Protect Bit	Block Protect Bit	Block Protect Bit	Write Enable Latch	Erase/Write In Progress
Reserved	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Volatile, Read Only	Volatile, Read Only

Status Register-2

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	WPS	Reserved	LB2	LB1	SUS2	QE	ADS
Erase Suspend	Write Protection Selection	Reserved	Security Register Lock Bit	Security Register Lock Bit	Program Suspend	Quad Enable	Current Address Mode
Volatile, Read Only	Non-volatile	Reserved	Non-volatile Writable (OTP)	Non-volatile Writable (OTP)	Volatile, Read Only	QE=1 fixed	Volatile, Read Only

Status Register-3

S23	S22	S21	S20	S19	S18	S17	S16
Reserved	DRV1	DRV0	ADP	EE	PE	LC	Reserved
Reserved	Output Driver Strength	Output Driver Strength	Power Up Address Mode	Erase Error bit	Program Error bit	Latency Code	Reserved
Reserved	Non-volatile	Non-volatile	Non-volatile	Volatile, Read Only	Volatile, Read Only	Non-volatile Writable	Reserved

Extended Address Register

EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0
Reserved	Reserved	Reserved	Reserved	DLP	Reserved	Reserved	A24
Reserved	Reserved	Reserved	Reserved	Data Learning Pattern Enable Bit	Reserved	Reserved	Address Bit
Reserved	Reserved	Reserved	Reserved	Volatile Writable	Reserved	Reserved	Volatile Writable

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP3, BP2, BP1, BP0 bits.

The Block Protect (BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table 1) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands.

T/B bit.

The Top/Bottom (TB) bit is a non-volatile bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as“0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

ADS bit.

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-Byte address mode when ADS=0 (default), and in 4-Byte address mode when ADS=1.

QE bit.

The Quad Enable (QE) bit is set to 1 by default in the factory, therefore the device supports Standard/Dual SPI as well as Quad SPI after power on. This bit cannot be reset to 0.

SUS1, SUS2 Bit.

The SUS1 and SUS2 bits are read only bit in the status register (S15 and S10) that are set to 1 after executing a Program/Erase Suspend (75H) command (The Erase Suspend will set the SUS1to 1, and the Program Suspend will set the SUS2to 1). The SUS1 and SUS2 bits are cleared to 0 by Program/Erase Resume (7AH) command, software reset (66H+99H) command as well as a power-down, power-up cycle.

LB1, LB2 bits.

The LB1, LB2, bits are non-volatile One Time Program (OTP) bits in Status Register (S11-S12) that provide the write protect control and status to the Security Registers. The default state of LB1-LB2 are 0, the security registers are unlocked. The LB1-LB2 bits can be set to 1 individually using the Write Register instruction. The LB1-LB2 bits are One Time Programmable, once being set to 1, the corresponding Security Register will become read-only permanently.

WPS bit.

The WPS Bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of T/B, BP (3:0) bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

Note: When WPS=1, Global Block Unlock(98H) command is needed before executing chip erase operation.

LC bit.

The Latency Code (LC) selects the mode and number of dummy cycles between the end of address and the start of read data output for command 0DH under QPI mode and command EDH under SPI/QPI modes.

Some read commands send mode bits following the address to indicate that the next command will be of the same type with an implied, rather than an explicit instruction. The next command thus does not provide an instruction Byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands.

Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional latency cycles as the SCLK frequency is increased.

Latency Code and DTR Mode Frequency Table

LC	Dummy clock cycles
0	8 (Default)
1	6

PE bit.

The Program Error (PE) bit is a read only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space.

Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

Note: The PE Error bits can only be accessed when WIP=0. The PE Error bits can also be reset at the next program operation.

EE bit.

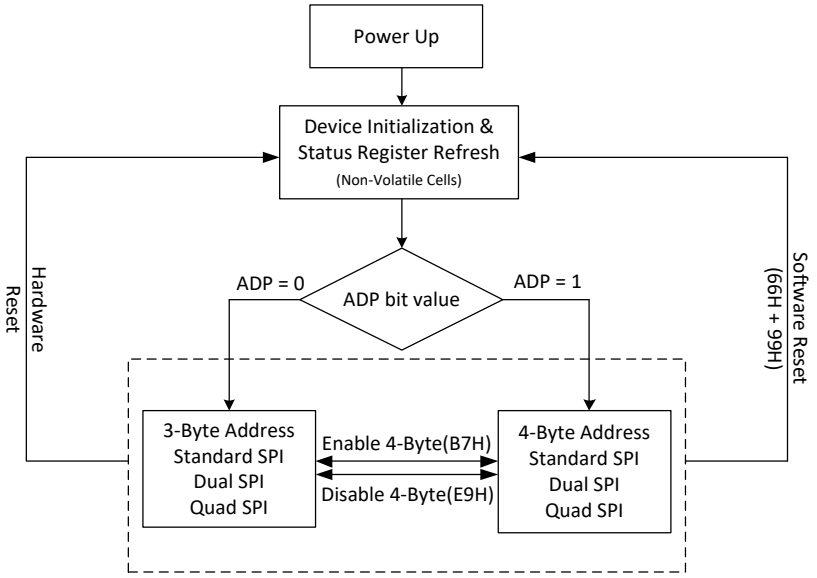
The Erase Error (EE) bit is a read only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space.

Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

Note: The EE Error bits can only be accessed when WIP=0. The EE Error bits can also be reset at the next erase operation.

ADP bit.

The Address Power-up (ADP) bit is a non-volatile writable bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period. When ADP=0(factory default), the device will power up into 3-Byte address mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte address mode directly.



DRV1, DRV0 bits

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1	DRV0	Driver Strength
0	0	25%
0	1	50%
1	0	75% (Default)
1	1	100%

Address bit.

The Extended Address Bit A24 is used only when the device is operating in the 3-Byte Address Mode (ADS=0), which is volatile writable by C5H command. The lower 128Mb memory array (0000 0000H – 00FF FFFFH) is selected when A24=0, and all instructions with 3-Byte addresses will be executed within that region. When A24=1, the upper 128Mb memory array (0100 0000H – 01FF FFFFH) will be selected. The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). Bits A31-A25 are reserved for higher densities.

If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7H)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Bit A24 setting will be ignored. However, any instruction with 4-Byte address input will replace the Extended Address Bit A24 with new settings.

A24	Address Range
0	0000 0000H – 00FF FFFFH
1	0100 0000H – 01FF FFFFH

DLP bit.

The DLP bit is Data Learning Pattern Enable bit. For Quad DTR Read commands, a pre-defined “Data Learning Pattern” can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins. When DLP=1, during the last 4 dummy clocks just prior to the data output, the flash will output “00110100” Data Learning Pattern sequence on each of the 4 I/O pins. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0 will disable the Data Learning Pattern output. The user defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to its “00110100” default value.

4. DATA PROTECTION

The device provides the following data protection methods:

- Write Enable (WREN) command: The WREN command sets the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up / Software Reset (66H + 99H)
  - Write Disable (WRDI)
  - Write Status Register (WRSR) / Write Extended Ad-dress Register (WEAR)
  - Page Program (PP) / Quad Page Program (QPP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
  - Erase Security Register / Program Security Register
- Software Protection Mode: The Block Protect (T/B, BP3, BP2, BP1, BP0) bits and WPS bit define the section of the memory array that can be read but cannot be changed.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command (ABH) and software reset (66H+99H).

Table 1. Protected Area Sizes

Protected Area Sizes (T/B bit = 0, WPS = 0)

Status bit				Protect Level
BP3	**BP2**	**BP1**	**BP0**	**256Mb**
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 511st)
0	0	1	0	2 (2 blocks, protected block 510th-511st)
0	0	1	1	3 (4 blocks, protected block 508th-511st)
0	1	0	0	4 (8 blocks, protected block 504th-511st)
0	1	0	1	5 (16 blocks, protected block 496th-511st)
0	1	1	0	6 (32 blocks, protected block 480th-511st)
0	1	1	1	7 (64 blocks, protected block 448th-511st)
1	0	0	0	8 (128 blocks, protected block 384th-511st)
1	0	0	1	9 (256 blocks, protected block 256th-511st)
1	0	1	0	10 (512 blocks, protected all)
1	0	1	1	11 (512 blocks, protected all)
1	1	0	0	12 (512 blocks, protected all)
1	1	0	1	13 (512 blocks, protected all)
1	1	1	0	14 (512 blocks, protected all)
1	1	1	1	15 (512 blocks, protected all)

Protected Area Sizes (T/B bit = 1, WPS = 0)

Status bit				Protect Level
BP3	**BP2**	**BP1**	**BP0**	**256Mb**
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0^{th})
0	0	1	0	2 (2 blocks, protected block 0^{th}-1^{st})
0	0	1	1	3 (4 blocks, protected block 0^{th}-3^{rd})
0	1	0	0	4 (8 blocks, protected block 0^{th}-7^{th})
0	1	0	1	5 (16 blocks, protected block 0^{th}-15^{th})
0	1	1	0	6 (32 blocks, protected block 0^{th}-31^{st})
0	1	1	1	7 (64 blocks, protected block 0^{th}-63^{rd})
1	0	0	0	8 (128 blocks, protected block 0^{th}-127^{th})
1	0	0	1	9 (256 blocks, protected block 0^{th}-255^{th})
1	0	1	0	10 (512 blocks, protected all)
1	0	1	1	11 (512 blocks, protected all)
1	1	0	0	12 (512 blocks, protected all)
1	1	0	1	13 (512 blocks, protected all)
1	1	1	0	14 (512 blocks, protected all)
1	1	1	1	15 (512 blocks, protected all)

Individual Block Protection (WPS=1)

<table>
<tr><th>Block</th><th>Sector</th><th colspan="2">Address range</th><th>Individual Block Lock Operation</th></tr>
<tr><td rowspan="3">511</td><td>8191</td><td>01FFFF00H</td><td>01FFFFFFH</td><td rowspan="10">The Top/Bottom block is protected by sector.

Other 510 Blocks are protected by block

Block Lock:
36H+Address
Block Unlock:
39H+Address
Read Block Lock:
3DH+Address
Global Block Lock:
7EH
Global Block Unlock:
98H</td></tr>
<tr><td>……</td><td>……</td><td>……</td></tr>
<tr><td>8176</td><td>01FF0000H</td><td>01FF00FFH</td></tr>
<tr><td>……</td><td colspan="3"></td></tr>
<tr><td>……</td><td colspan="3"></td></tr>
<tr><td>2</td><td colspan="3"></td></tr>
<tr><td>1</td><td colspan="3"></td></tr>
<tr><td rowspan="3">0</td><td>15</td><td>00F000H</td><td>00FFFFH</td></tr>
<tr><td>……</td><td>……</td><td>……</td></tr>
<tr><td>0</td><td>000000H</td><td>000FFFH</td></tr>
</table>

5. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See the table below, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable or Write Disable command, CS# must be driven high exactly at the byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 2. Commands

Command Name	Command Code	SPI	QPI	Address Byte					Dummy Cycle	Data Byte
				Total ADD Byte	Byte1	Byte2	Byte3	Byte4		
Register Access										
Read Status Register_1	05H	√	√	0					0	1 to ∞
Read Status Register_2	35H	√	√	0					0	1 to ∞
Read Status Register_3	15H	√	√	0					0	1 to ∞
Write Status Register_1	01H	√	√	0					0	1
Write Status Register_2	31H	√	√	0					0	1
Write Status Register_3	11H	√	√	0					0	1
Read Extended Address Register	C8H	√	√	0					0	1 to ∞
Write Extended Address Register	C5H	√	√	0					0	1
Manufacturer/Device ID	90H	√	√	3	ADD1	ADD2	ADD3		0	1 to ∞
Manufacturer/Device ID by Dual I/O	92H	√		3	ADD1	ADD2	ADD3		4 Note3	1 to ∞
Manufacturer/Device ID by Quad I/O	94H	√		3	ADD1	ADD2	ADD3		6 Note3	1 to ∞
Read Serial Flash Discoverable Parameters	5AH	√	√	3	ADD1	ADD2	ADD3		8 Note1	1 to ∞
Read Unique ID	4BH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8 Note1	1 to 128bit
Read Identification	9FH	√	√	0					0	1 to ∞
Array access										
Read Data	03H	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to ∞

Fast Read	0BH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8 Note1	1 to ∞
Dual Output Fast Read	3BH	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to ∞
Dual I/O Fast Read	BBH	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	4 Note3	1 to ∞
Quad Output Fast Read	6BH	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to ∞
Quad I/O Fast Read	EBH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	6 Note1 Note3	1 to ∞
Quad I/O Word Fast Read	E7H	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	4 Note3	1 to ∞
4-Byte Read	13H	√		4	ADD1	ADD2	ADD3	ADD4	0	1 to ∞
4-Byte Fast Read	0CH	√	√	4	ADD1	ADD2	ADD3	ADD4	8 Note1	1 to ∞
4-Byte Dual Output Fast Read	3CH	√		4	ADD1	ADD2	ADD3	ADD4	8	1 to ∞
4-Byte Dual I/O Fast Read	BCH	√		4	ADD1	ADD2	ADD3	ADD4	4 Note3	1 to ∞
4-Byte Quad Output Fast Read	6CH	√		4	ADD1	ADD2	ADD3	ADD4	8	1 to ∞
4-Byte Quad I/O Fast Read	ECH	√	√	4	ADD1	ADD2	ADD3	ADD4	6 Note1 Note3	1 to ∞
4-Byte DTR Quad I/O Fast Read	EEH	√	√	4	ADD1	ADD2	ADD3	ADD4	8 Note1 Note3	1 to ∞
DTR Fast Read	0DH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	6	1 to ∞
DTR Fast Read Dual I/O	BDH	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	6 Note3	1 to ∞
DTR Fast Read Quad I/O	EDH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8 Note1 Note3	1 to ∞
Page Program	02H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
Quad Page Program	32H	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
Extended Quad Input Fast Program	C2H	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
4-Byte Page Program	12H	√	√	4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
4-Byte Quad Input Fast Program	34H	√		4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
4-Byte Quad Input Extended Fast Program	3EH	√		4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
4KB Sector Erase	20H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
32KB Block Erase	52H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
64KB Block Erase	D8H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Chip Erase	C7/60H	√	√	0					0	0
4-Byte 4KB Sector Erase	21H	√	√	4	ADD1	ADD2	ADD3	ADD4	0	0
4-Byte 32KB Block Erase	5CH	√	√	4	ADD1	ADD2	ADD3	ADD4	0	0

4-Byte 64KB Block Erase	DCH	√	√	4	ADD1	ADD2	ADD3	ADD4	0	0
Device Operations										
Enable Reset	66H	√	√	0					0	0
Reset	99H	√	√	0					0	0
Write Enable	06H	√	√	0					0	0
Write Enable for Volatile Status Register	50H	√	√	0					0	0
Write Disable	04H	√	√	0					0	0
Program Erase Suspend	75H	√	√	0					0	0
Program Erase Resume	7AH	√	√	0					0	0
Enable QPI	38H	√		0					0	0
Disable QPI	FFH		√	0					0	0
Set Burst with Wrap	77H	√		0					0	0
Set Read Parameters	C0H		√	0					0	0
Enter 4-Byte Address Mode	B7H	√	√	0					0	0
Exit 4-Byte Address Mode	E9H	√	√	0					0	0
Clear Flag Status Register Command	30H	√	√	0					0	0
Continuous Read Reset	FFH[Note2]	√	√							
Deep Power-Down	B9H	√	√	0					0	0
Release From Deep Power-Down/Read Device ID	ABH	√	√	0					24	0
One-Time Programmable (OTP) Operations										
Read Security Register	48H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to ∞
Program Security Register	42H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
Erase Security Register	44H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Advanced Sector Protection Operations										
Global Block Lock	7EH	√	√	0					0	0
Global Block Unlock	98H	√	√	0					0	0
Individual Block Lock	36H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Individual Block Unlock	39H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Read Block Lock	3DH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1

Note1:

The number of dummy clocks for 0BH/0CH/EBH/ECH/5AH/4BH under QPI mode will be configured as either 8/4/6 (default = 8) by the “Set Read Parameters (C0H)” command.

The number of dummy clocks for 0DH_QPI/EDH/EEH/EDH_QPI/EEH_QPI will be configured as either 8/6 (default = 8) by LC bit in status register.

Note2:

Under SPI mode and Continuous Read Mode, Command FFH will exit the Continuous Read mode.

Under QPI mode and Continuous Read Mode, the first time sending command FFH will exit the Continuous Read mode, and the second time sending FFH will exit QPI mode.

Note3:

M7-0 is counted for dummy clocks.

Table of Device ID Definitions:

XT25BF256B

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	0B	40	19
90H	0B		18
ABH			18

5.1. Register Access

5.1.1. Read Status Register (05H/35H/15H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. For the command code “35H”, the SO will output Status Register bits S15~S8. For the command code “15H”, the SO will output Status Register bits S23~S16.

Figure 1. Read Status Register Sequence Diagram

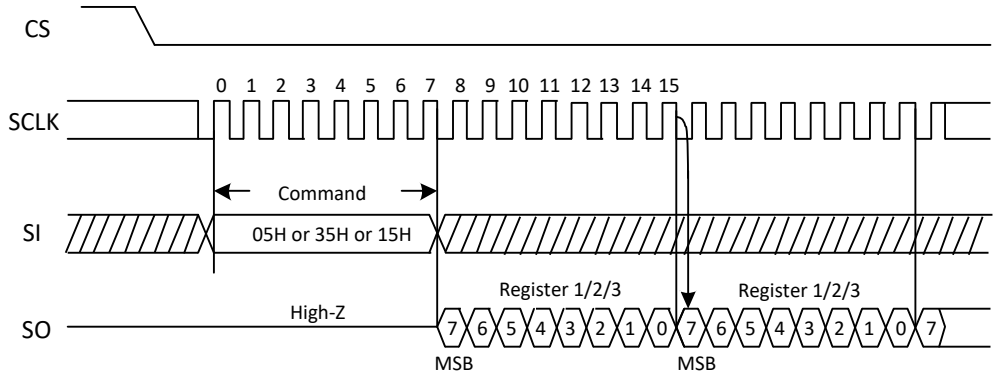
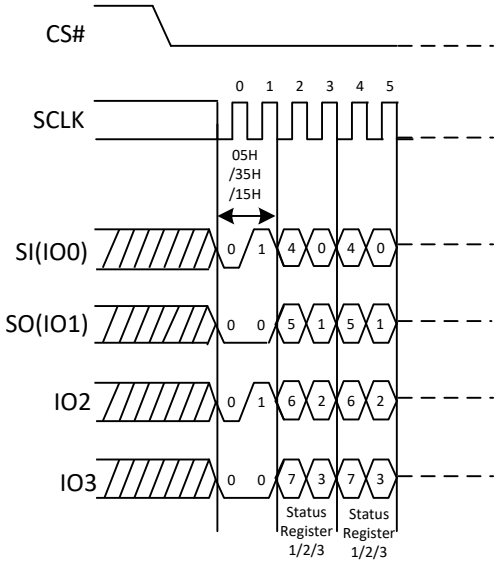


Figure 1a. Read Status Register Sequence Diagram (QPI)



5.1.2. Write Status Register (01H/31H/11H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on the volatile bits of the Status Register. CS# must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (T/B, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in the Protected Area Sizes table. For command code “01H”, the SI will input Status Register bits S7~S0. For the command code “31H”, the SI will input Status Register bits S15~S8. For the command code “11H”, the SI will input Status Register bits S23~S16.

Figure 2. Write Status Register Sequence Diagram

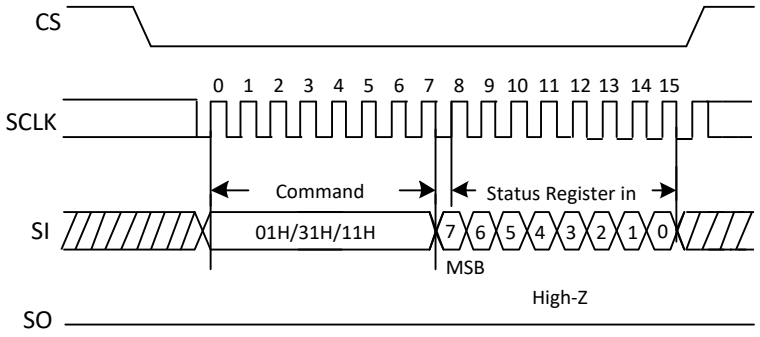
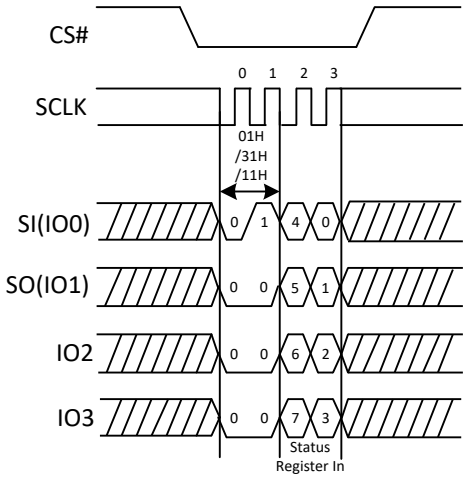


Figure 2a. Write Status Register Sequence Diagram (QPI)



5.1.3. Read Extended Address Register (C8H)

Extended Address Register contains Address Bits A31-A24. The Read Extended Address Register instruction is entered by driving CS# low and shifting the instruction code "C8H" into the SI pin on the rising edge of SCLK. The Extended Address Register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first.

When the device is in the 4-Byte Address Mode, the value of A31-A24 bits is ignored.

Figure 3. Read Extended Address Register Diagram

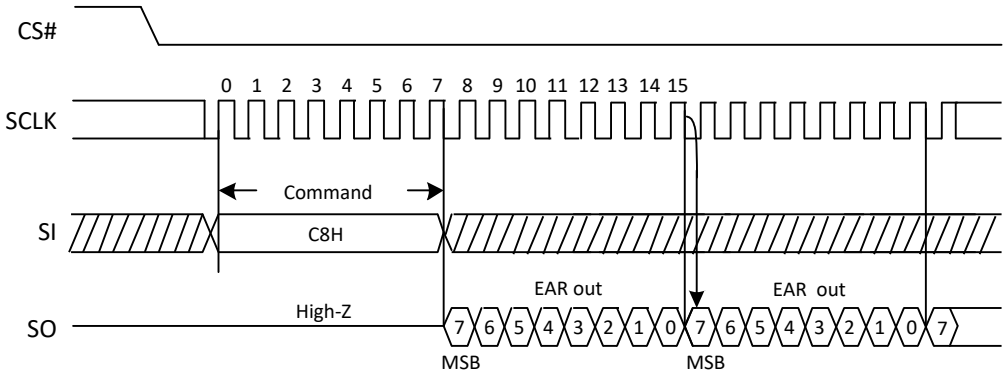
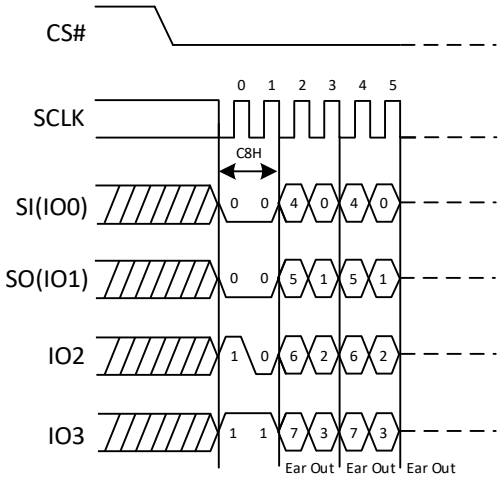


Figure 3a. Read Extended Address Register Diagram (QPI)



5.1.4. Write Extended Address Register (C5H)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction. Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “C5H”, and then writing the Extended Address Register data byte.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Register is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any command with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

Figure 4. Write Extended Address Register Diagram

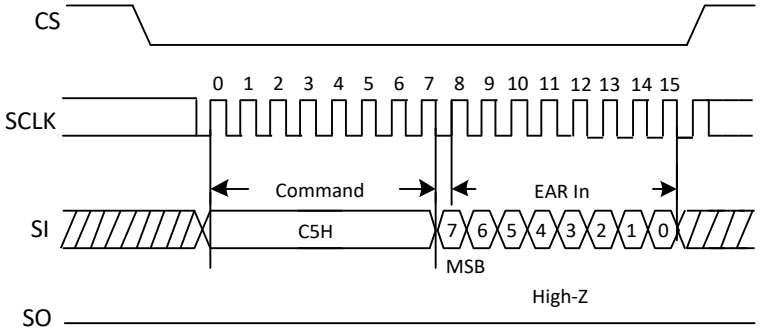
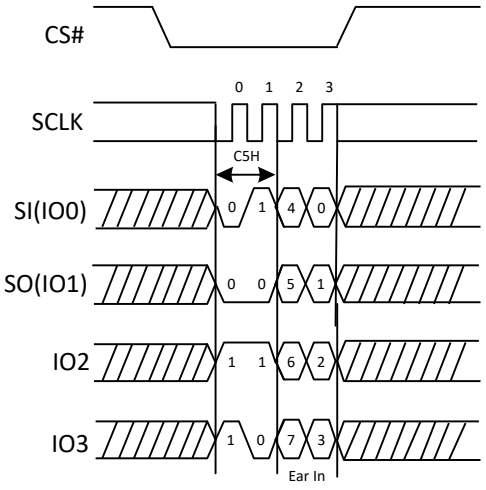


Figure 4a. Write Extended Address Register Diagram (QPI)



5.1.5. Read Manufacture ID/ Device ID (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Deep Power-Down and Read Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in the figure below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 5. Read Manufacture ID/ Device ID Sequence Diagram

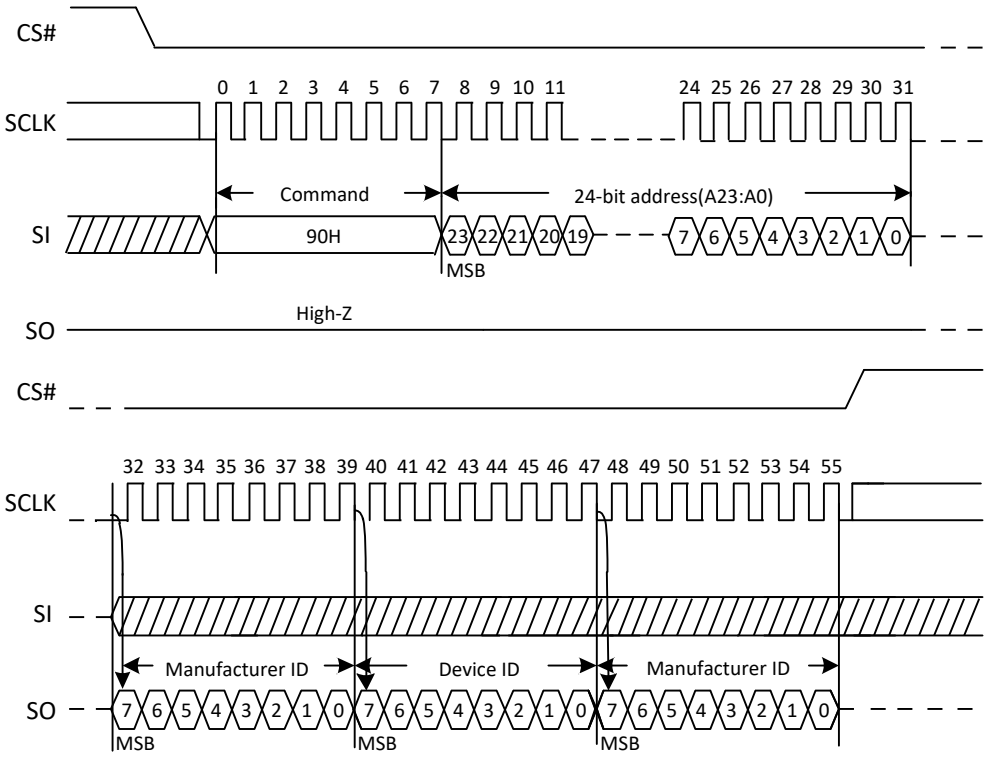
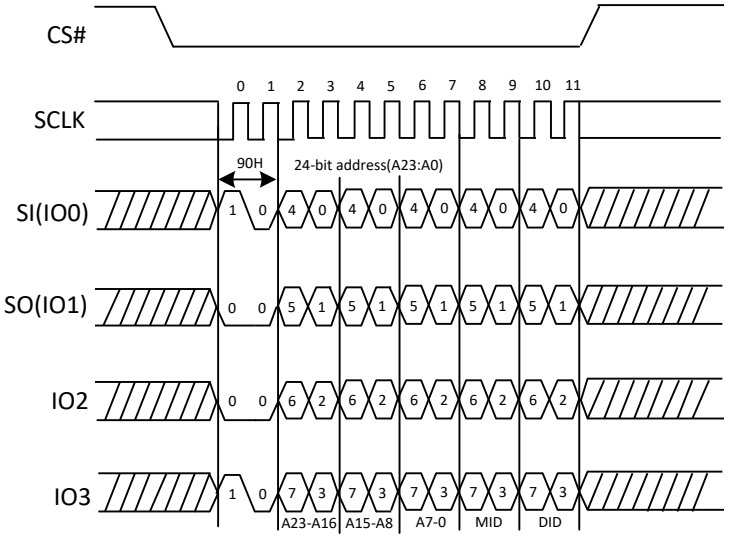


Figure 5a. Read Manufacture ID/ Device ID Sequence Diagram (QPI)

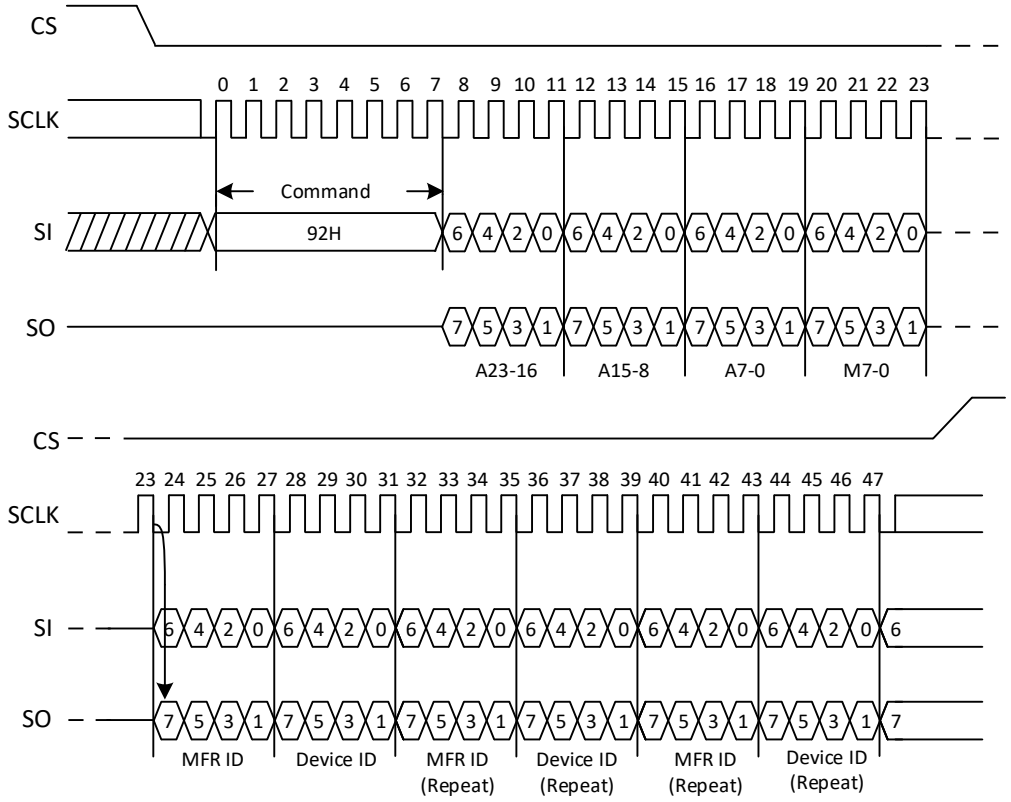


5.1.6. Read Manufacture ID/ Device ID Dual I/O (92H)

The Read Manufacturer/Device ID Dual I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the CS# pin low and shifting the command code “92H” followed by a 24-bit address (A23-A0) of 000000H and M7-M0. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in the figure below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

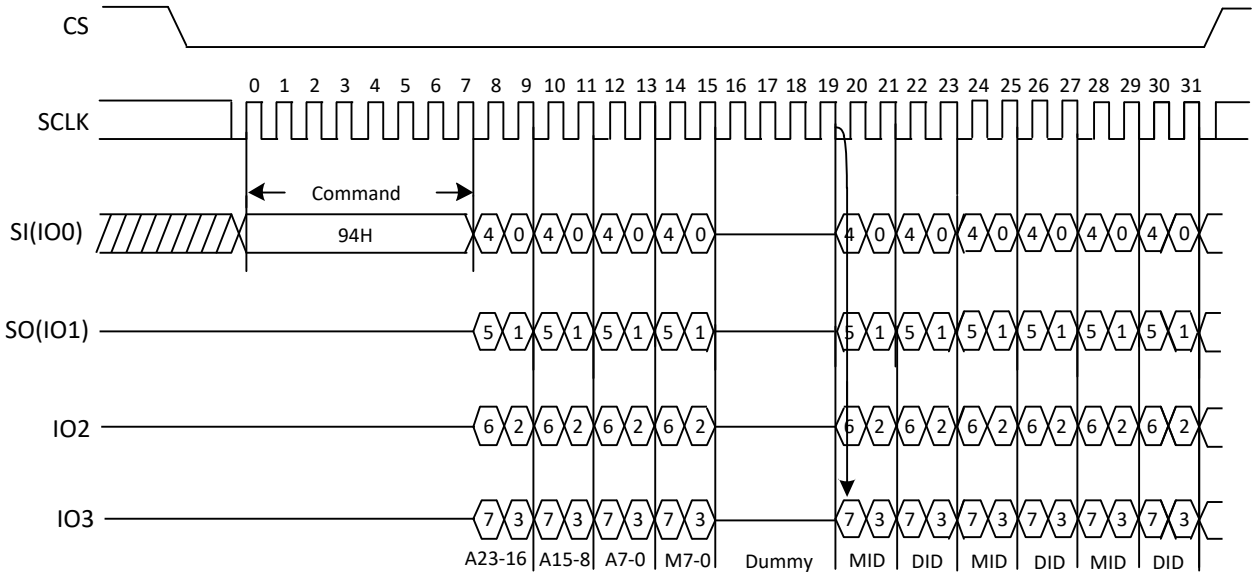
Figure 6. Read Manufacture ID/ Device ID Dual I/O Sequence Diagram



5.1.7. Read Manufacture ID/ Device ID Quad I/O (94H)

The Read Manufacturer/Device ID Quad I/O command is an alternative to the Release from Deep Power-Down and Read Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O. The command is initiated by driving the CS# pin low and shifting the command code "94H" followed by a 24-bit address (A23-A0) of 000000H and 6 dummy clocks (M7-M0 included). After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in the figure below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 7. Read Manufacture ID/ Device ID Quad I/O Sequence Diagram

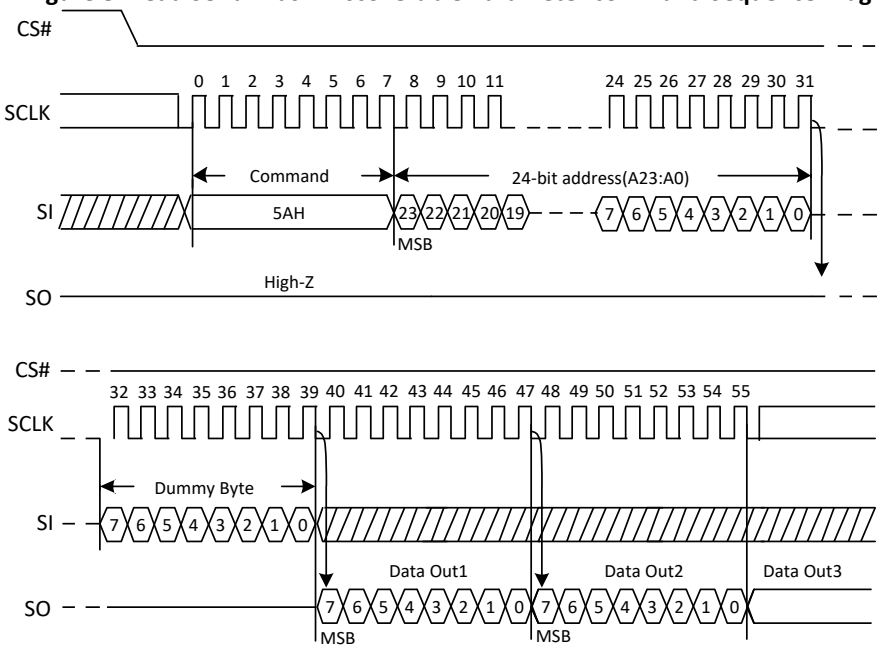


5.1.8. Read SFDP (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

Note: For detail information, please contact with XTX.

Figure 8. Read Serial Flash Discoverable Parameter command Sequence Diagram

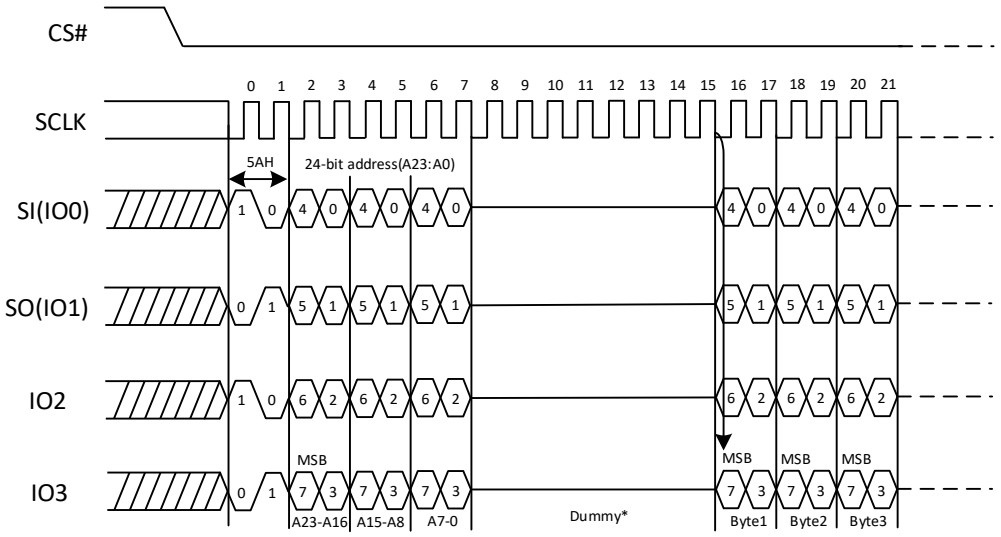


Note1: A23-A8 = 0, A7-A0 is the starting byte address for 256-byte SFDP Register.

Read Serial Flash Discoverable Parameter (5AH) in QPI mode

The Read Serial Flash Discoverable Parameter command is also supported in QPI mode. See the following figure. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Figure 8a. Read Serial Flash Discoverable Parameter command Sequence Diagram (QPI)



*Set Read Parameters Command (C0H) can set the number of dummy clocks

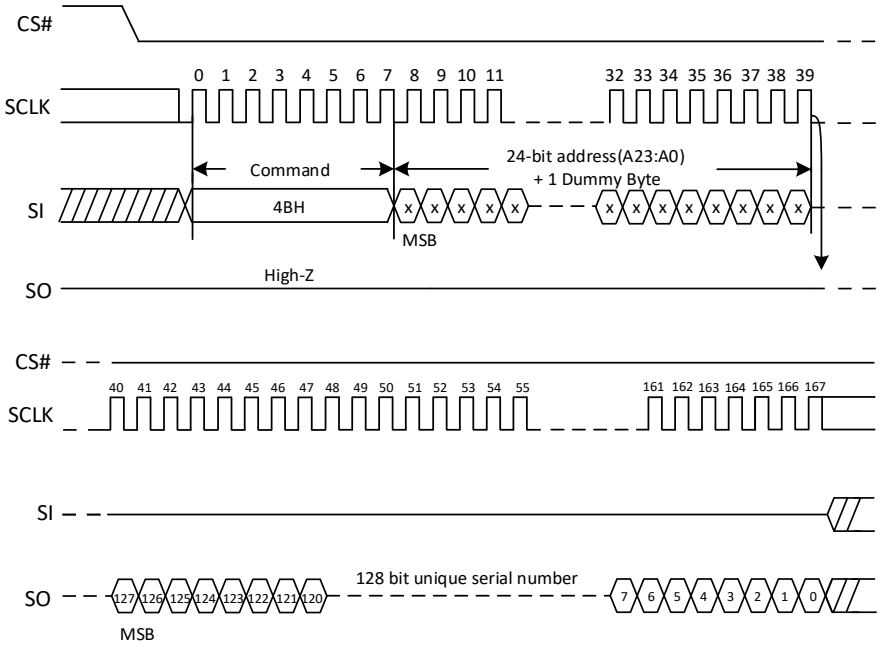
5.1.9. Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command →sending 24-bit address (A23:A0) (Don't care) + 1 dummy Byte → 128bit Unique ID Out → CS# goes high.

The command sequence is shown below.

Figure 9. Read Unique ID (RUID) Sequence (Command 4BH)

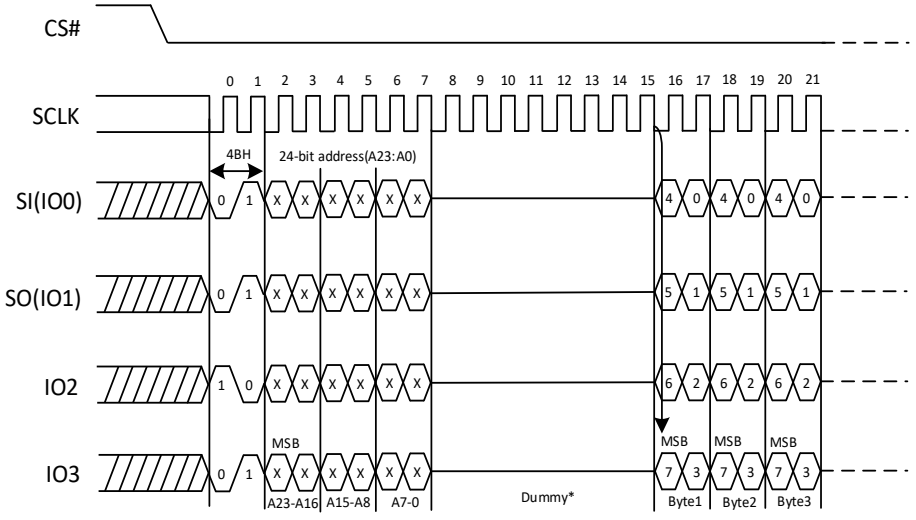


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Read Unique ID (4BH) in QPI mode

The Read Unique ID command is also supported in QPI mode. See the figure below, In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Figure 9a. Read Unique ID (RUID) Sequence (Command 4BH) (QPI)



*Set Read Parameters Command (C0H) can set the number of dummy clocks

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.1.10. Read Identification (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress will not be decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit manufacture identification and device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in the figure below. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 10. Read Identification ID Sequence Diagram

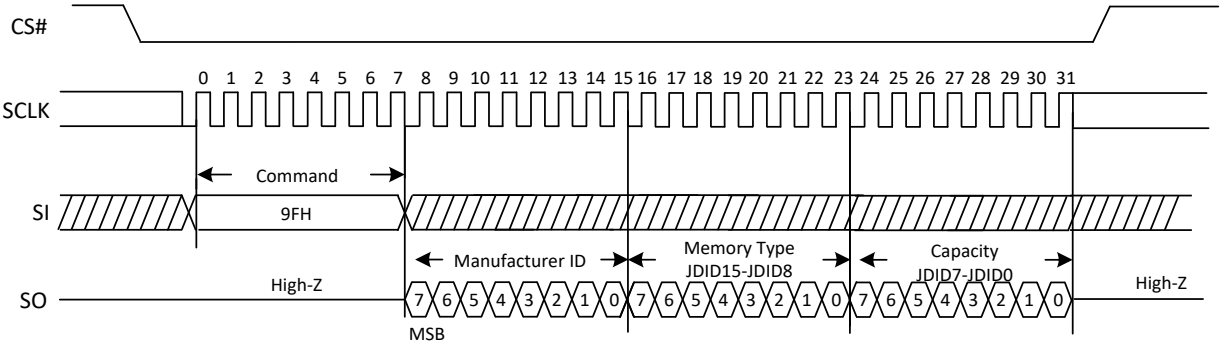
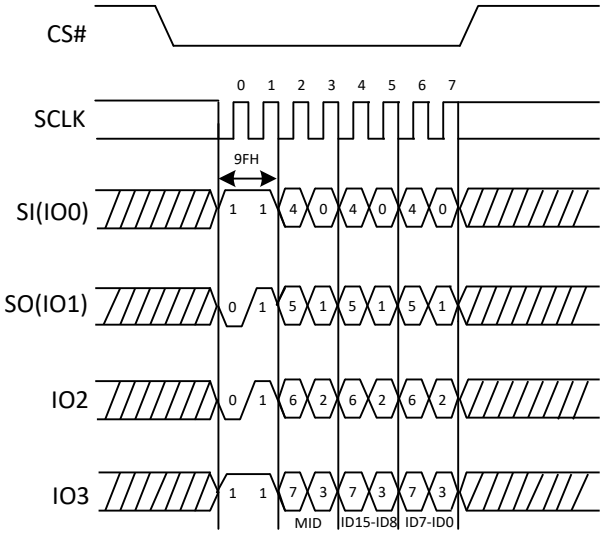


Figure 10a. Read Identification ID Sequence Diagram (QPI)

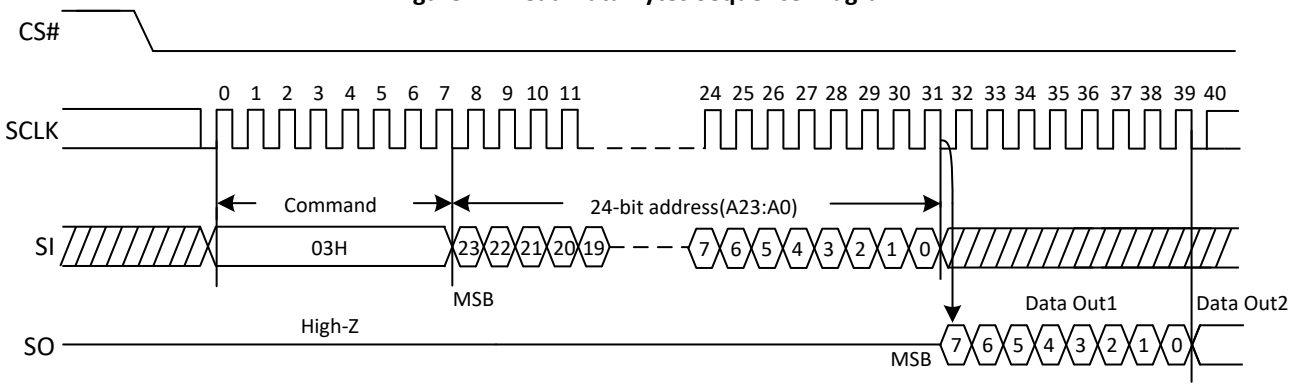


5.2. Array Access

5.2.1. Normal Read (03H/13H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0) or a 4-byte address (A31-A0), and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fR, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 11. Read Data Bytes Sequence Diagram

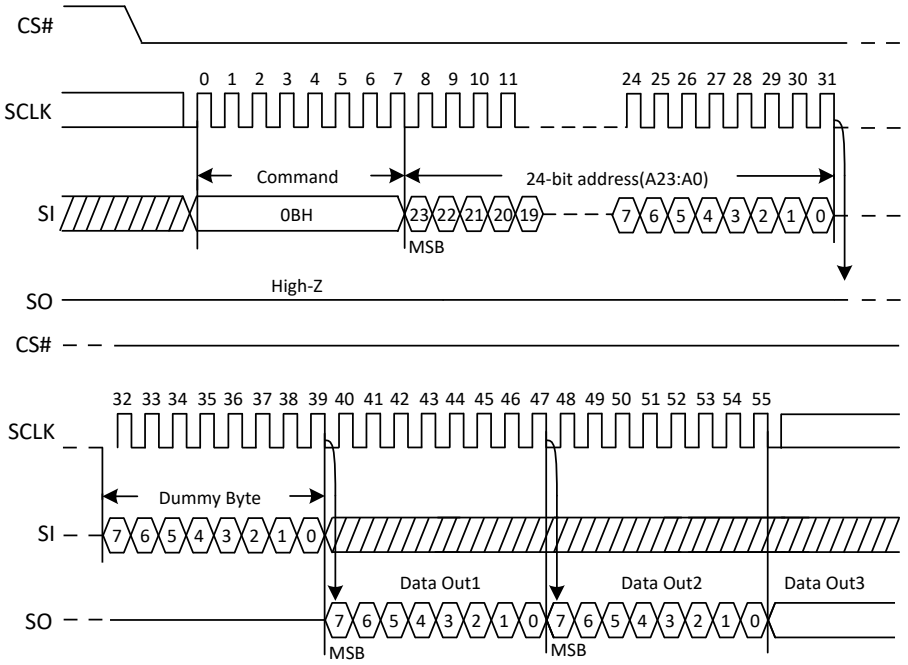


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.2. Fast Read (0BH/0CH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) or a 4-byte address (A31-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fC, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 12. Read Data By test Higher Speed Sequence Diagram

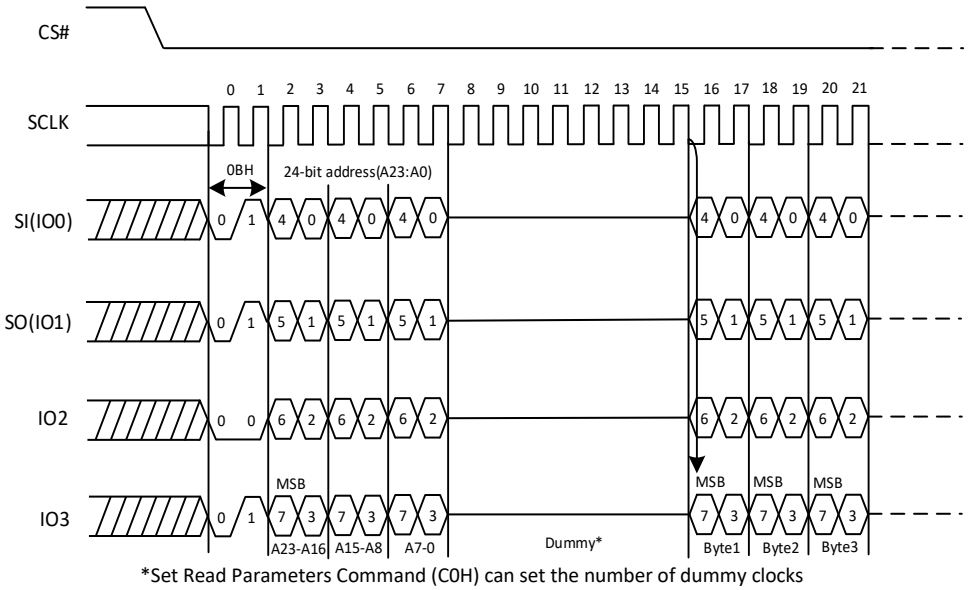


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Fast Read (0BH) in QPI mode

The Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Figure 12a. Read Data Bytes at Higher Speed Sequence Diagram (QPI)



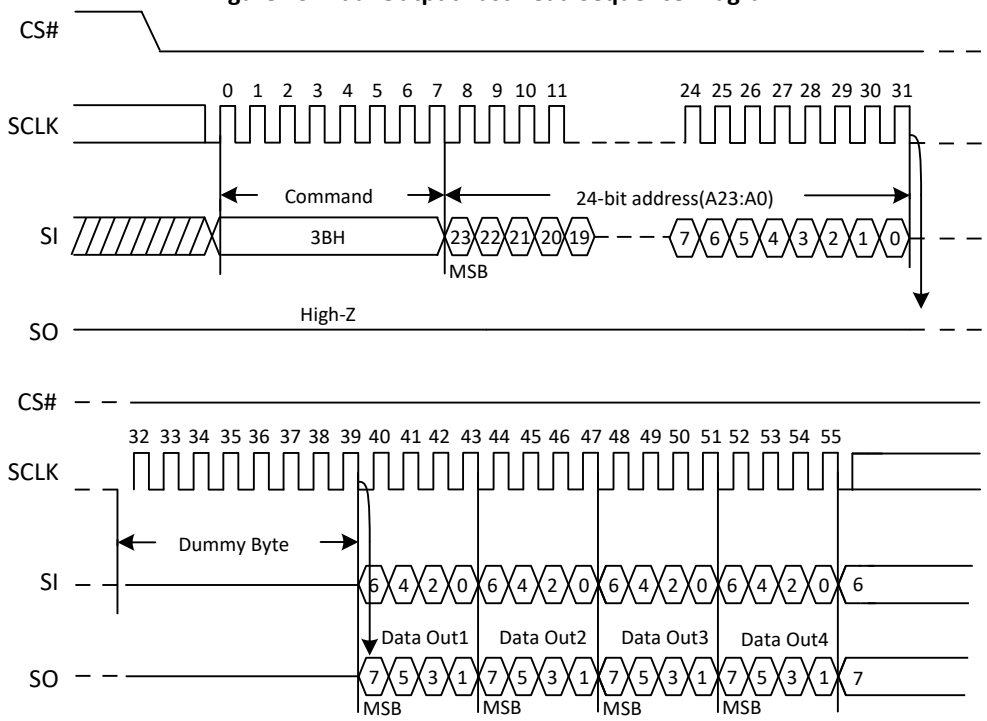
*Set Read Parameters Command (C0H) can set the number of dummy clocks

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.3. Dual Output Fast Read (3BH/3CH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) or a 4-byte address (A31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in the figure below. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 13. Dual Output Fast Read Sequence Diagram

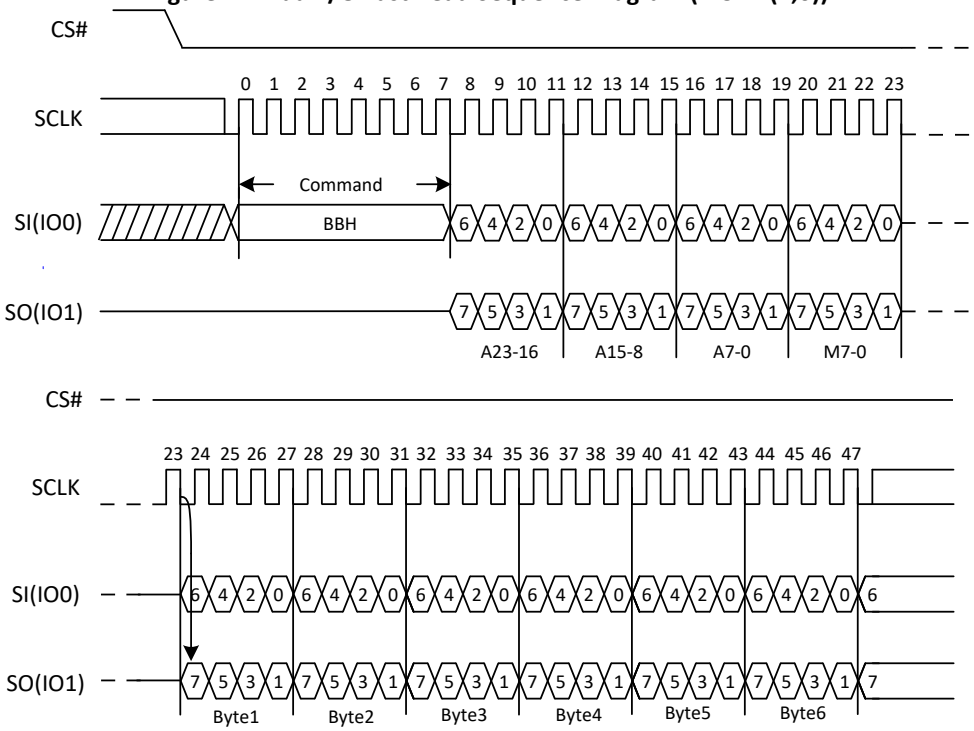


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.4. Dual I/O Fast Read (BBH/BCH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input a 3-byte address (A23-0) or a 4-byte address (A31-A0) and the "Continuous Read Mode" bits (M7-M0) 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in the figure below. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 14. Dual I/O Fast Read Sequence Diagram (M5-4≠(1,0))

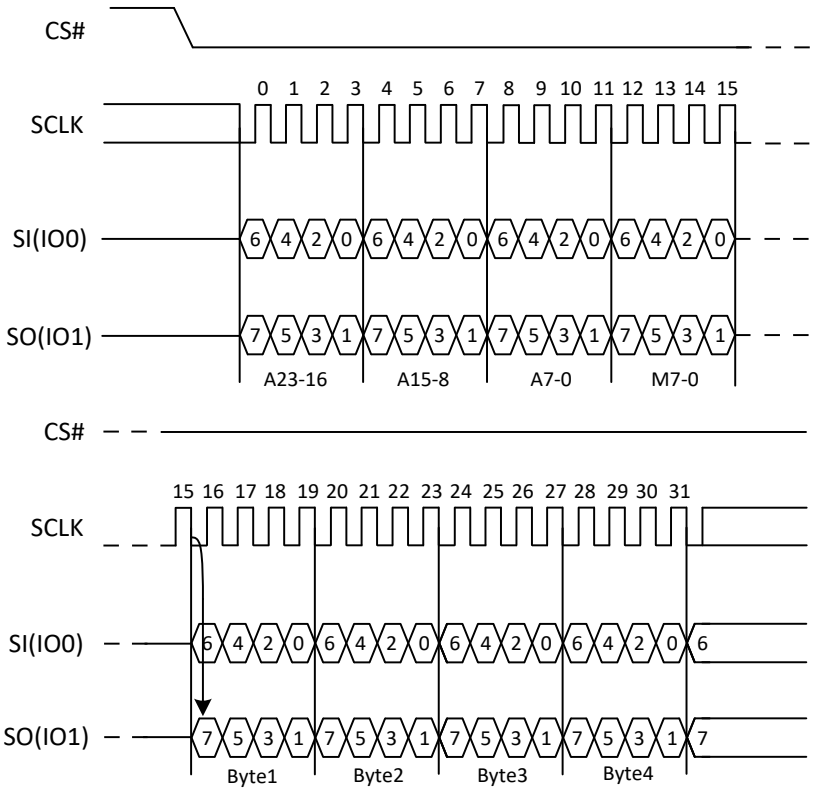


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Dual I/O Fast Read with "Continuous Read Mode"

The Dual I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0) or a 4-byte address (A31-A0). If the "Continuous Read Mode" bits (M5- 4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in the figure below. If the "Continuous Read Mode" bits (M5- 4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5- 4) before issuing normal command.

Figure 14a. Dual I/O Fast Read Sequence Diagram (M5-4=(1,0))

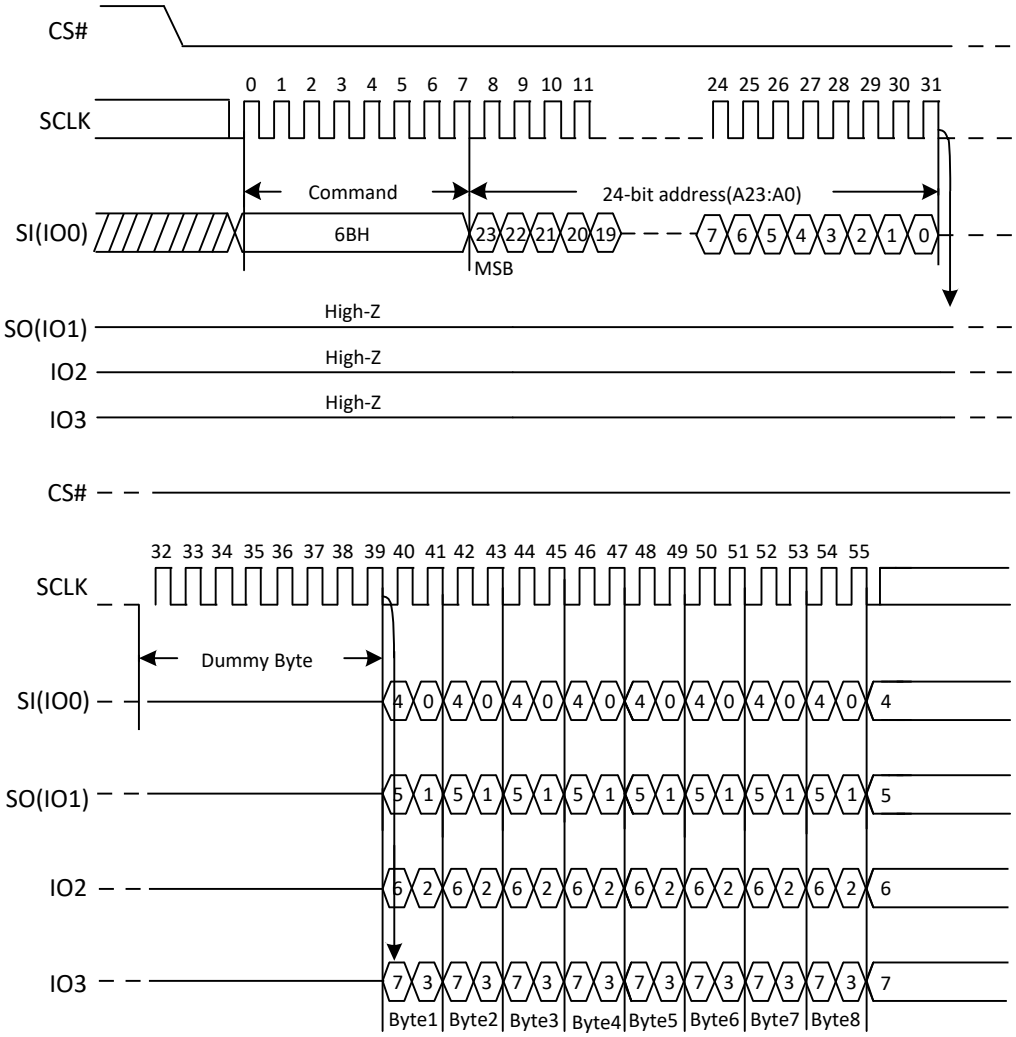


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.5. Quad Output Fast Read (6BH/6CH)

The Quad Output Fast Read command is followed by a 3-byte address (A23-A0) or a 4-byte address (A31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in the figure below. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 15. Quad Output Fast Read Sequence Diagram

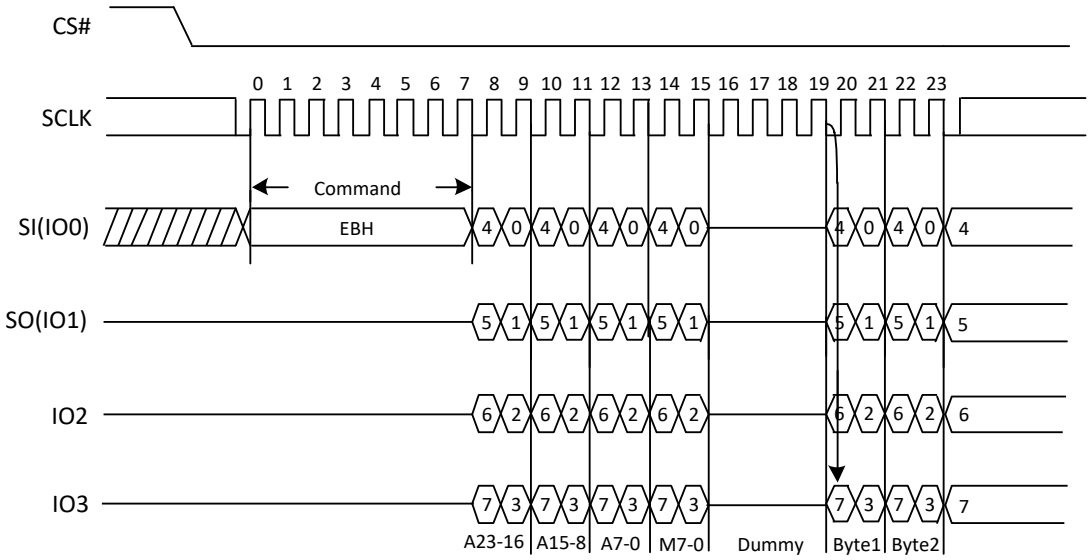


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.6. Quad I/O Fast Read (EBH/ECH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input a 3-byte address (A23-0) or a 4-byte address (A31-A0) and a "Continuous Read Mode" byte (M7-0) and 4 dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in the figure below. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 16. Quad I/O Fast Read Sequence Diagram (M5-4≠(1,0))

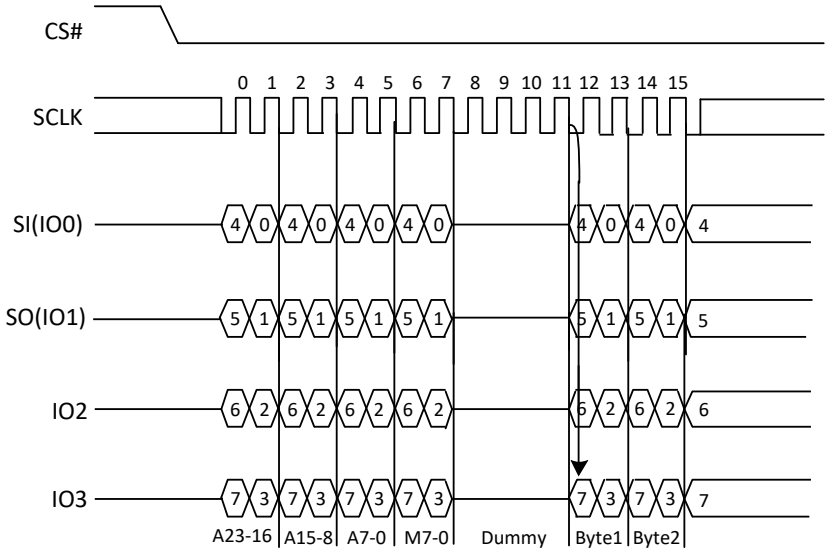


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Quad I/O Fast Read (EBH/ECH) with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0) or a 4-byte address (A31-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in the figure below. If the "Continuous Read Mode" (M5- 4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5- 4) before issuing normal command.

Figure 16a. Quad I/O Fast Read Sequence Diagram (M5-4=(1,0))



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Quad I/O Fast Read (EBH/ECH) with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

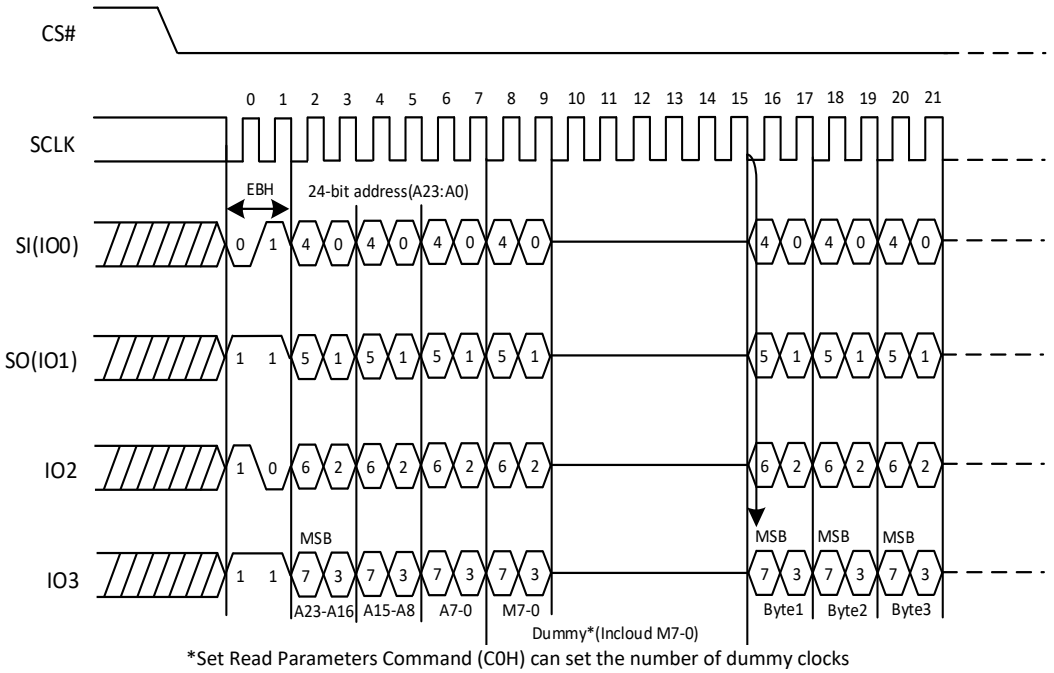
The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

Quad I/O Fast Read (EBH/ECH) in QPI mode

The Quad I/O Fast Read command is also supported in QPI mode. See the figure below. In QPI mode, the number of dummy clocks (8 dummy by default) is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8. In QPI mode, the "Continuous Read Mode" bits M7-M0 are also considered as dummy clocks. "Continuous Read Mode" feature is available in QPI mode for Quad I/O Fast Read command. The "Wrap Around" feature is also available in QPI mode for Quad I/O Fast Read command. The "Wrap Length" and the number of dummy clocks can be configured by the "Set Read Parameters (C0H)" command. Also "EDH" and "EEH" are alternative ways to perform "Wrap Around" under QPI mode.

Figure 16b. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0) QPI)



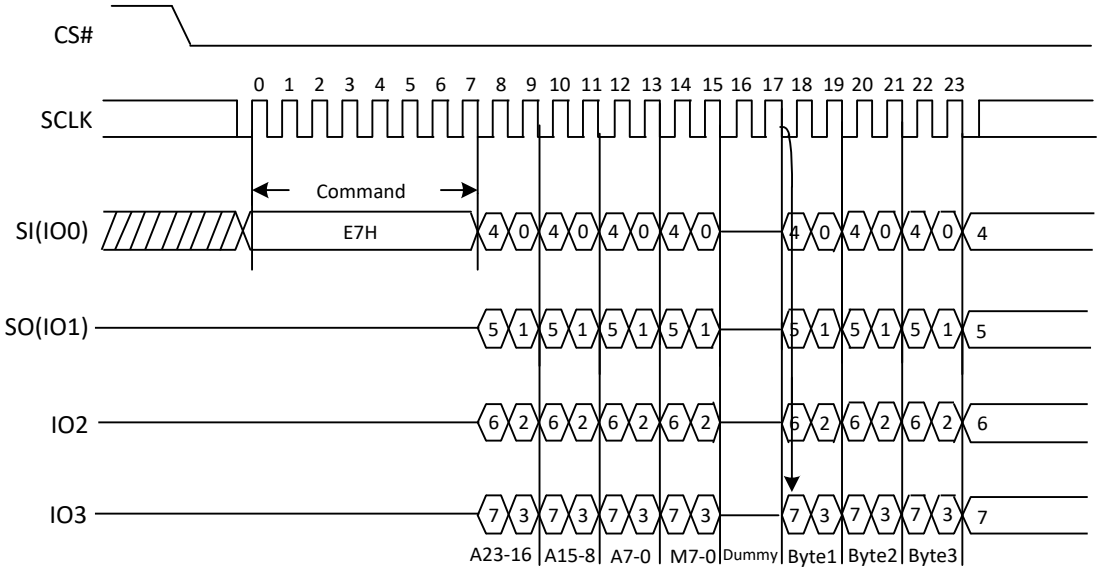
*Set Read Parameters Command (C0H) can set the number of dummy clocks

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.7. Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command input a 3-byte address (A23-0) or a 4-byte address (A31-A0) and the "Continuous Read Mode" bits (M7-0) and 2 dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, except that the lowest address bit (A0) must equal 0. The command sequence is shown in the figure below. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 17. Quad I/O Word Fast Read Sequence Diagram (M5-4≠(1,0))

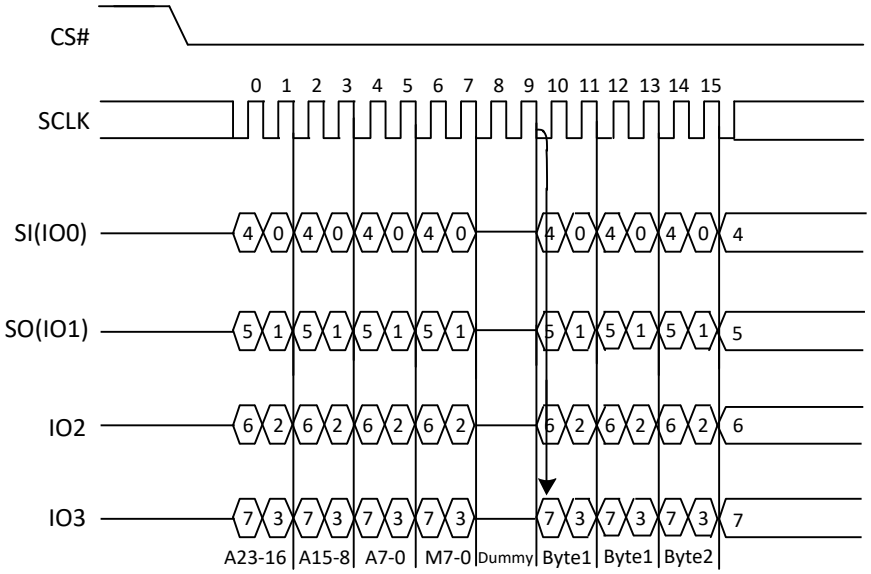


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) = (1, 0), then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in the figure below. If the "Continuous Read Mode" bits (M5- 4) do not equal (1, 0), the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-0) before issuing normal command.

Figure 17a. Quad I/O Word Fast Read Sequence Diagram (M5-4=(1,0))



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

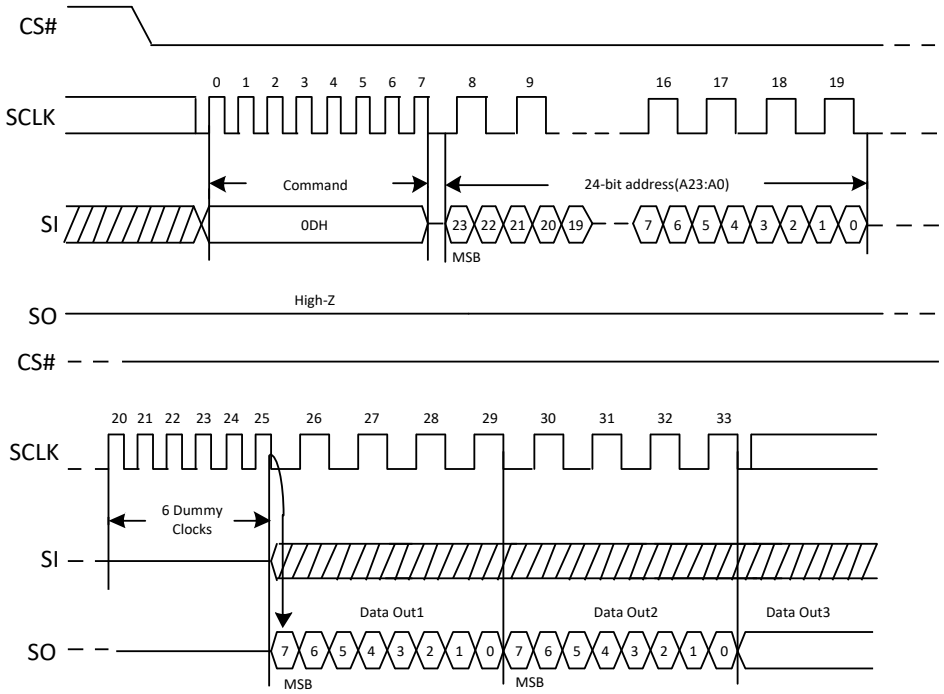
Quad I/O Word Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Word Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to E7H. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following E7H commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command. The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

5.2.8. DTR Fast Read (0DH)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24-bit or 32-byte address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding six dummy clocks after a 3-byte address (A23-A0) or a 4-byte address (A31-A0) as shown in the figure below. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the IO pin is a "don't care".

Figure 18. DTR Fast Read Instruction (SPI Mode)

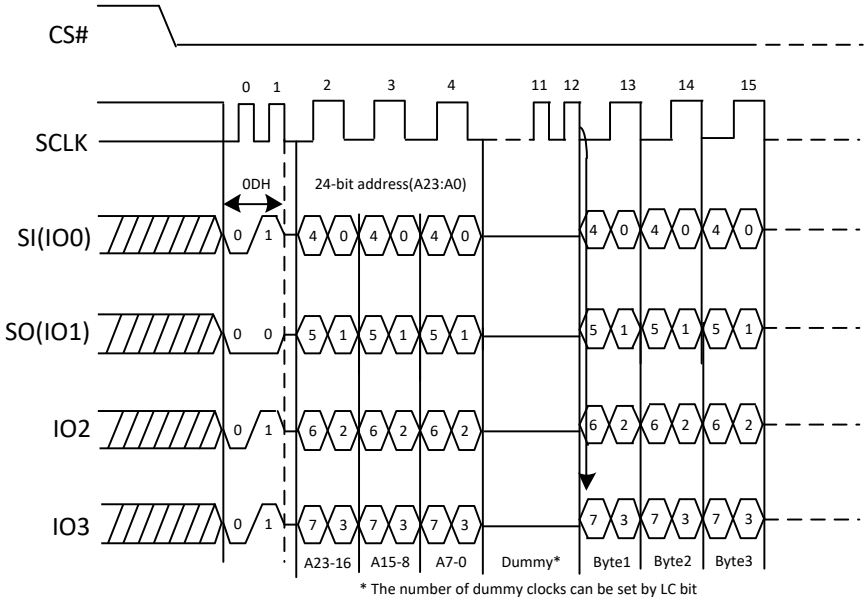


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

DTR Fast Read in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode. The number of dummy clocks for "DTR Fast Read" (0DH) under QPI mode and "DTR Fast Read Quad IO" (EDH) can be set by the Latency Code (LC) in status register. When the LC bit is set to 0, which is default, the number of dummy clock cycles is 8. When the LC bit is set to 1, the dummy clock cycles is 6.

Figure 18a. DTR Fast Read Instruction (QPI Mode)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.9. DTR Fast Read Dual I/O (BDH)

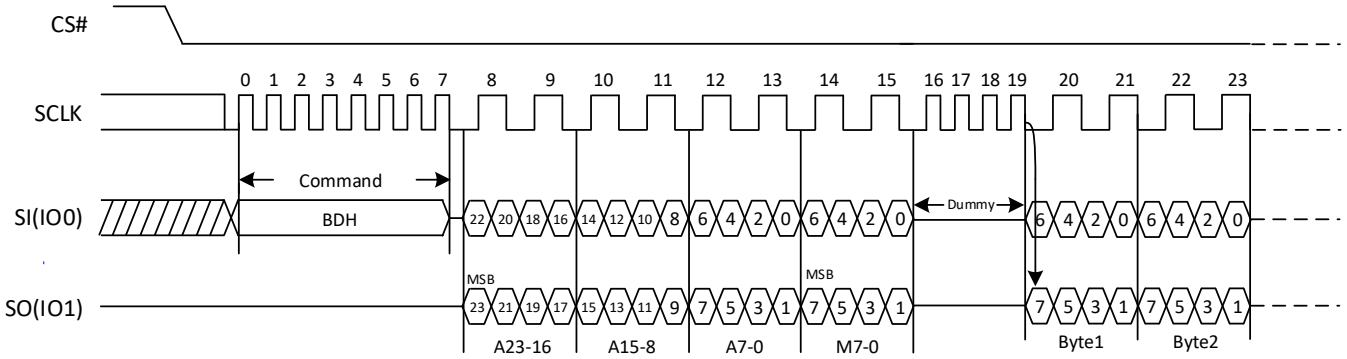
The DTR Fast Read Dual I/O (BDH) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3BH) instruction but with the capability to input a 3-byte address (A23-A0) or a 4-byte address (A31-A0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

DTR Fast Read Dual I/O with "Continuous Read Mode"

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after a 3-byte address (A23-A0) or a 4-byte address (A31-A0), as shown in "3BH" command description. The upper nibble of the (M7-4) controls the length of the next DTR Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance for 4 dummy clocks prior to the falling edge of the first data out clock.

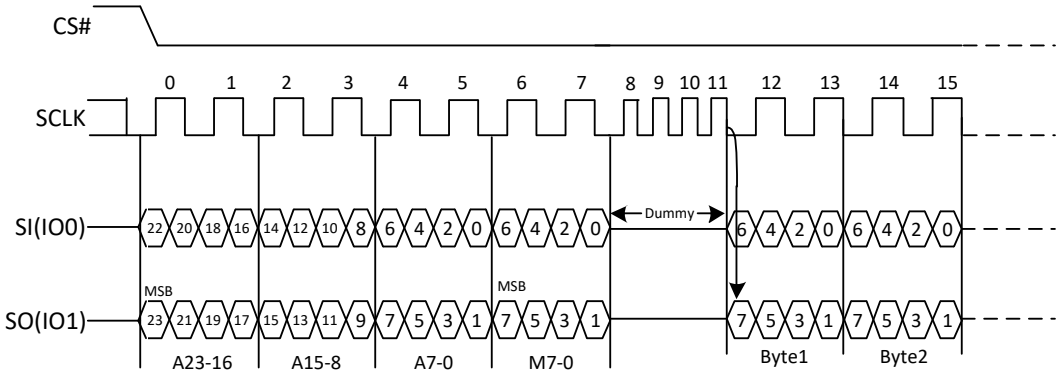
If the "Continuous Read Mode" bits M5-4 = (1, 0), then the next DTR Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BDH instruction code, as shown in the figure below. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFH/FFFFFH on IO0 for the next instruction (16/20 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 19. DTR Fast Read Dual I/O (Initial instruction or previous M5-4≠10, SPI Mode only)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 19a. DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.10. DTR Fast Read Quad I/O (EDH/EEH)

The DTR Fast Read Quad I/O (EDH) instruction is similar to the Fast Read Dual I/O (BBH) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and several Dummy clocks (including M7-M0) are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

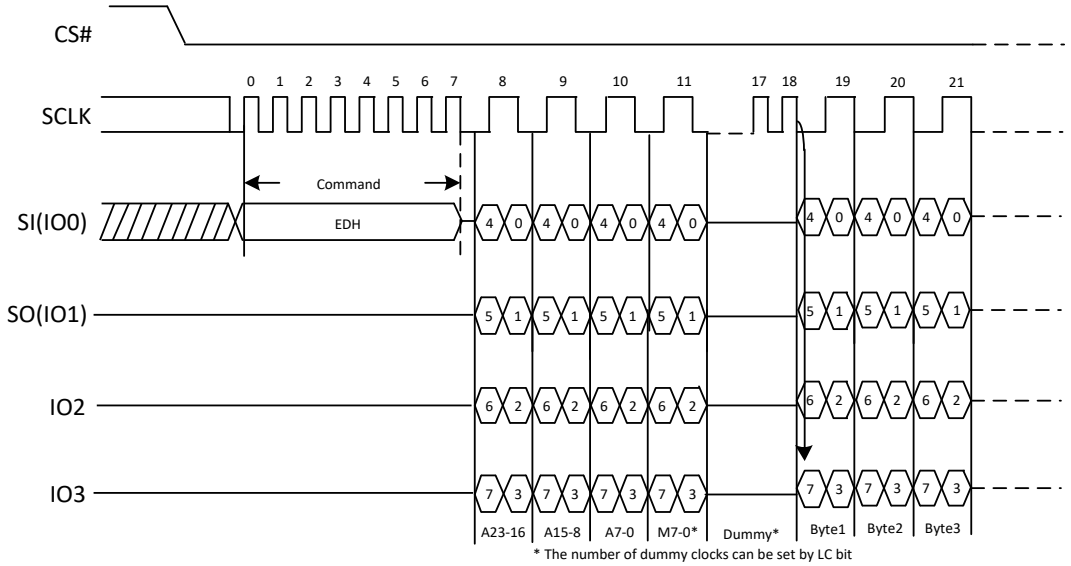
The number of dummy clocks for "DTR Fast Read" (0DH) under QPI mode and "DTR Fast Read Quad I/O" (EDH) under SPI and QPI mode can be set by the Latency Code (LC) in status register. When the LC bit is set to 0, which is default, the number of dummy clock cycles is 8. When the LC bit is set to 1, the dummy clock cycles is 6.

DTR Fast Read Quad I/O with "Continuous Read Mode"

The DTR Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after inputting the 3-byte address (A23-0) or a 4-byte address (A31-A0), as shown in "6BH" or "6CH" command description. The upper nibble of the (M7-4) controls the length of the next DTR Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

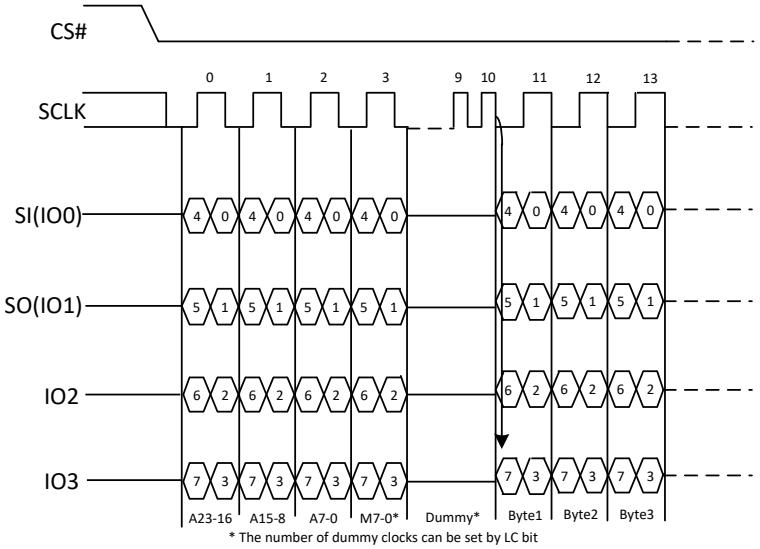
If the "Continuous Read Mode" bits M5-4 = (1,0), then the next DTR Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the EBH instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFH/3FFH on IO0 for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 20. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, SPI Mode)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 20a. DTR Fast Read Quad I/O (Previous instruction set M5-4=10, SPI Mode)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The DTR Fast Read Quad I/O command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EDH or EEH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EDH or EEH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

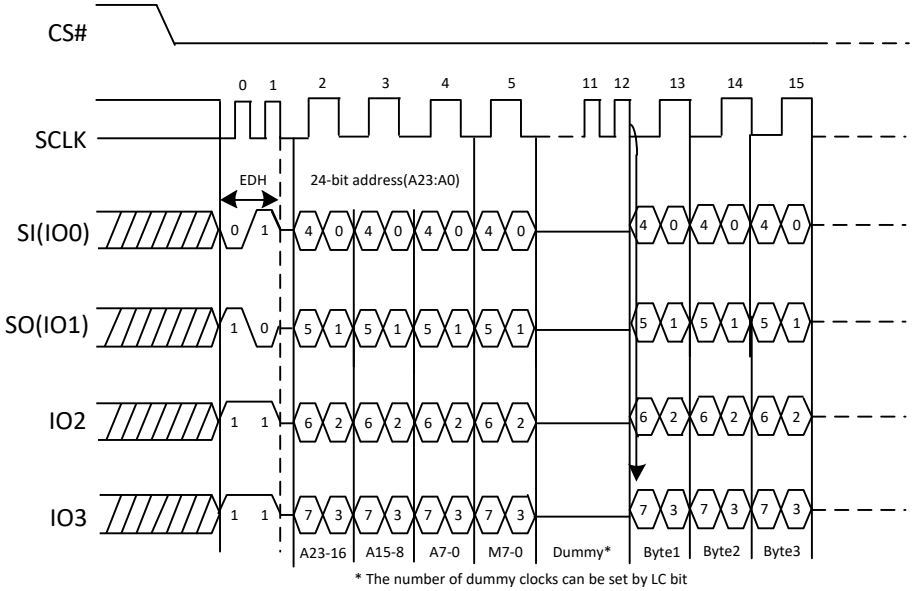
DTR Fast Read Quad I/O (EDH/EEH) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in the figure below. In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

The "Wrap Around" feature is also available in QPI mode for DTR Fast Read Quad I/O command. The "Wrap Length" can be configured by the "Set Read Parameters (C0H)" command. However, the number of dummy clocks is set by LC bit in status register and cannot be configured by the "Set Read Parameters (C0H)" command for DTR Fast Read Quad I/O instruction. Also "EBH" and "ECH" are alternative ways to perform "Wrap Around" under QPI mode.

"Continuous Read Mode" feature is also available in QPI mode for DTR Fast Read Quad I/O instruction. Please refer to the description on previous pages.

Figure 20b. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.11. Page Program (02H/12H)

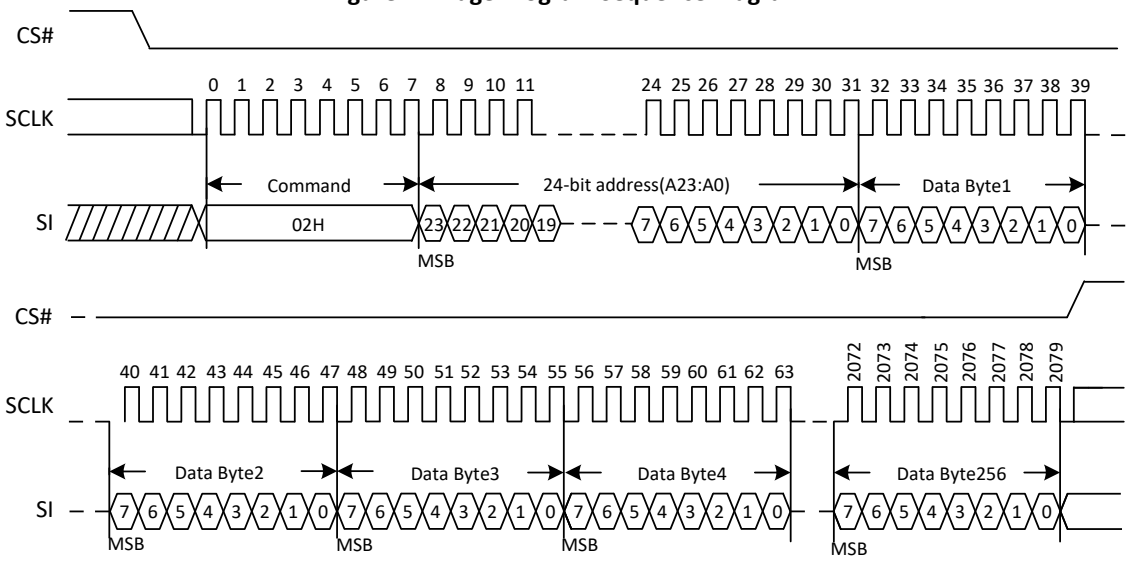
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low →sending Page Program command→ 3-byte address or 4-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in the figure below. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

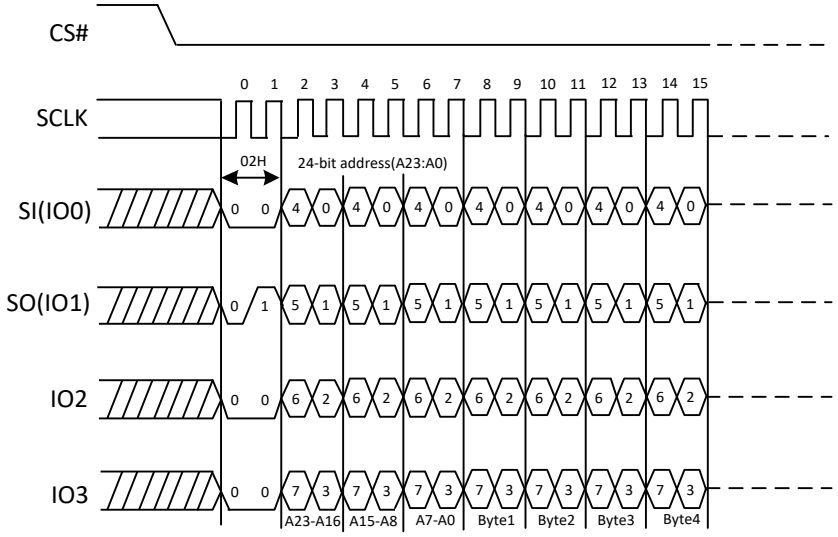
A Page Program (PP) command applied to a page which is protected by the Block Protect (T/B, BP3, BP2, BP1, BP0) is not executed.

Figure 21. Page Program Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 21a. Page Program Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.12. Quad Page Program (32H/34H)

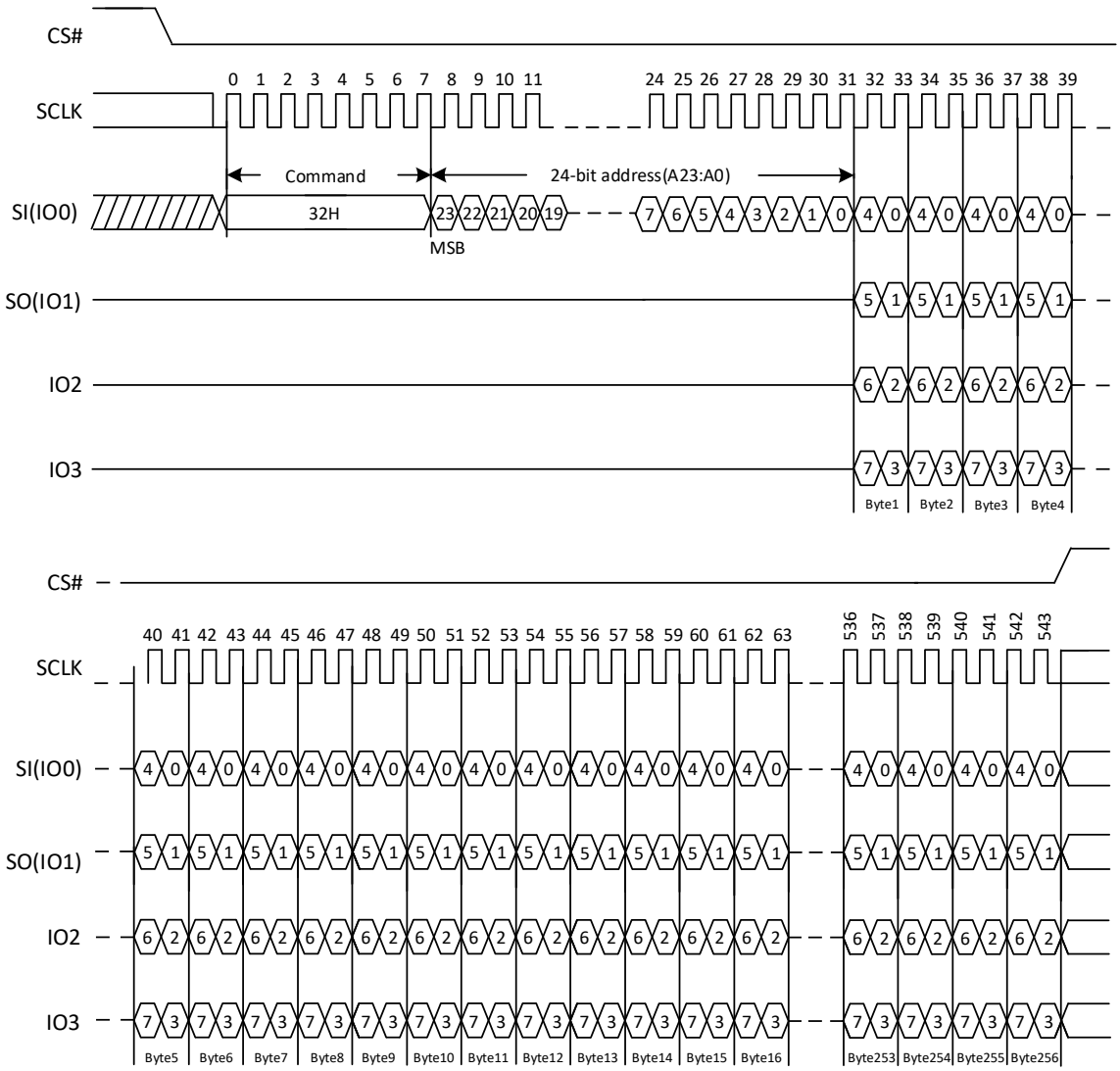
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The Quad Page Program command is entered by driving CS# Low, followed by the command code (32H/34H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in the figure below. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command will not be executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (T/B, BP3, BP2, BP1, BP0) will not be executed.

Figure 22. Quad Page Program Sequence Diagram



5.2.13. Extend Quad Page Program (C2H/3EH)

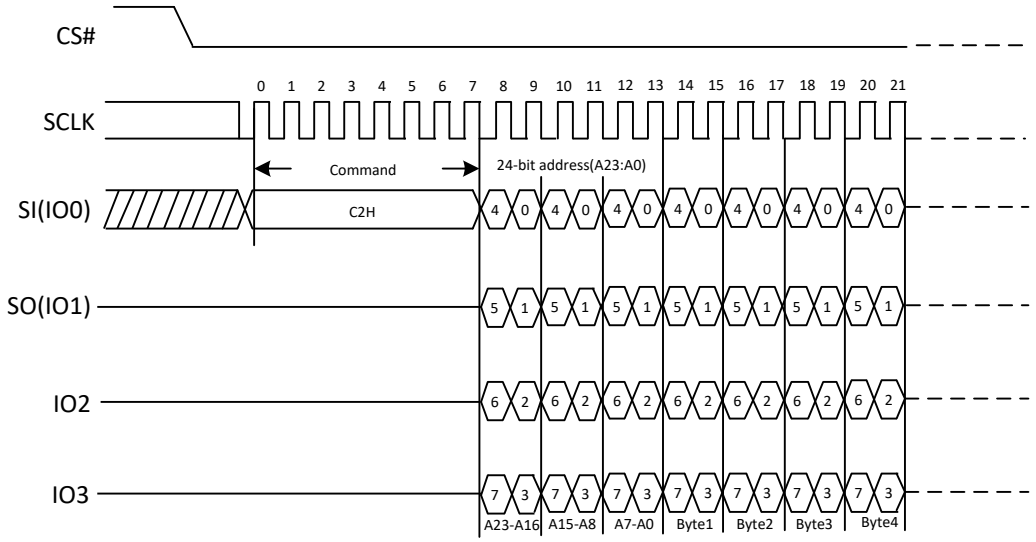
The Extend Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The extend quad Page Program command is entered by driving CS# Low, followed by the command code (C2H/3EH), three or four address bytes and at least one data byte on IO pins.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Extend Quad Page Program (EPP) command is not executed.

As soon as CS# is driven high, the self-timed Extend Quad Page Program cycle (whose duration is tPP) is initiated. While the Extend Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Extend Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

An Extend Quad Page Program command applied to a page which is protected by the Block Protect (T/B, BP3, BP2, BP1, and BP0) is not executed.

Figure 23. Extend Quad Page Program Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

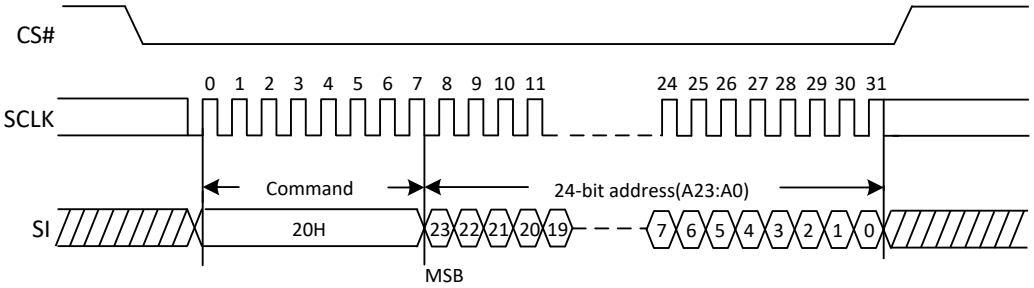
5.2.14. Sector Erase (20H/21H)

The Sector Erase (SE) command is for erasing all the data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Sector Erase command. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte or 4-byte address on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command.

The Sector Erase command sequence: CS# goes low→ sending Sector Erase command→ 3-byte address or 4-byte address on SI→ CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command will not be executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (T/B, BP3, BP2, BP1, BP0) bit will not be executed.

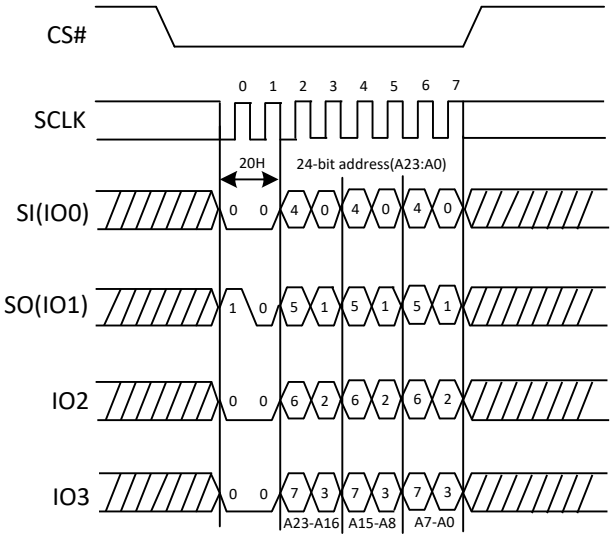
Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 24. Sector Erase Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 24a. Sector Erase Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

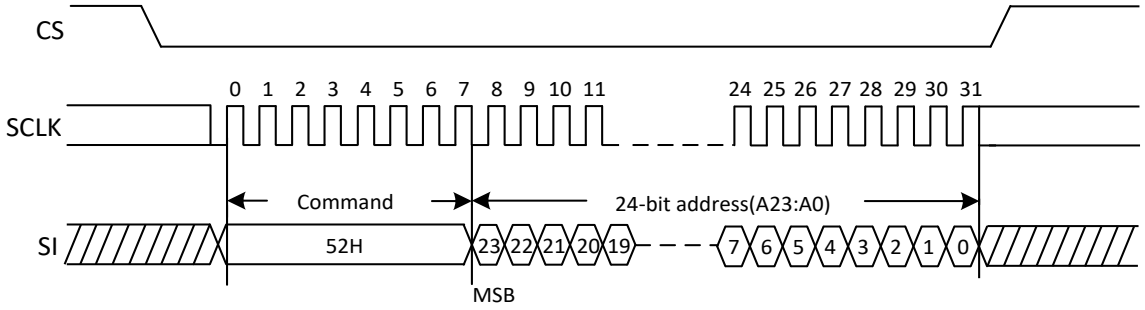
5.2.15. 32KB Block Erase (52H/5CH)

The 32KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the 32KB Block Erase command. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and 3 address bytes or 4-byte address on SI, driving CS# high. Any address inside the block is a valid address for the 32KB Block Erase (BE) command.

The 32KB Block Erase command sequence: CS# goes low→ sending 32KB Block Erase command→ 3-byte address or 4-byte address on SI→CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE1) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (T/B, BP3, BP2, BP1, BP0) bits will not be executed.

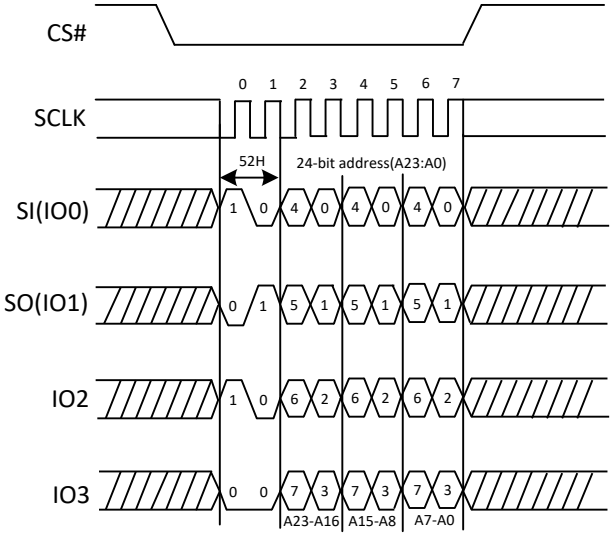
Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 25. 32KB Block Erase Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 25a. 32KB Block Erase Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

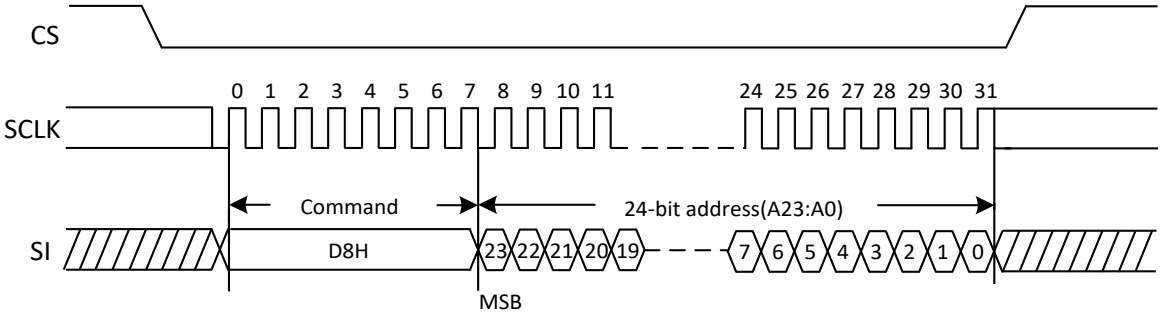
5.2.16. 64KB Block Erase (D8H/DCH)

The 64KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the 64KB Block Erase command. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and 3 address bytes or 4-byte address on SI, driving CS# high. Any address inside the block is a valid address for the 64KB Block Erase (BE) command.

The 64KB Block Erase command sequence: CS# goes low →sending 64KB Block Erase command→ 3-byte address or 4-byte address on SI→CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE2) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (T/B, BP3, BP2, BP1, BP0) bits will not be executed.

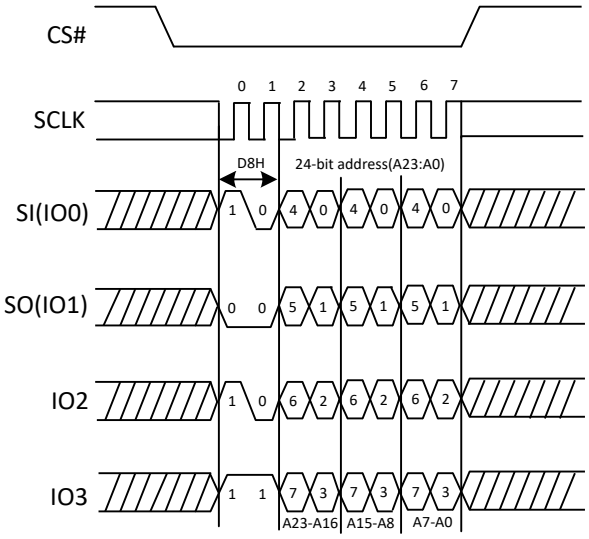
Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 26. 64KB Block Erase Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 26a. 64KB Block Erase Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.2.17. Chip Erase (60H/C7H)

The Chip Erase (CE) command is for erasing all the data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the Chip Erase command. The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI).

The Chip Erase command sequence: CS# goes low→ sending Chip Erase command→CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the command code has been latch in, otherwise the Chip Erase command will not be executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 27. Chip Erase Sequence Diagram

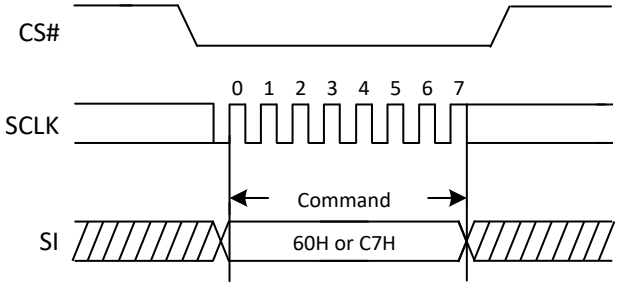
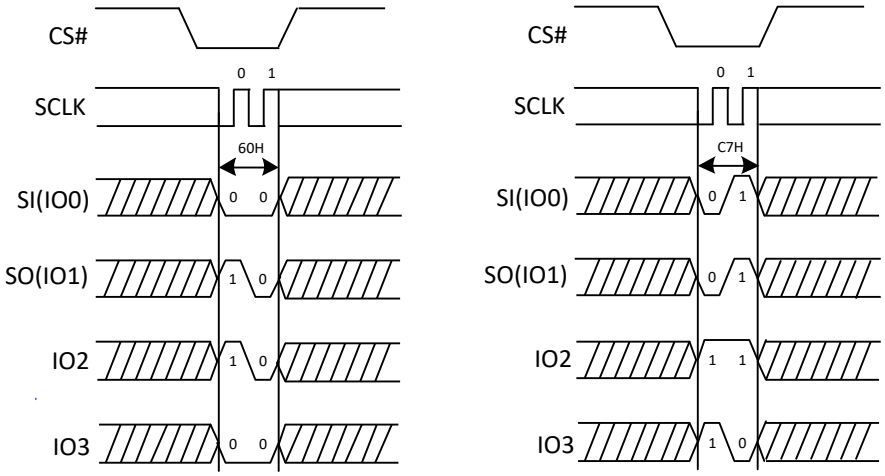


Figure 27a. Chip Erase Sequence Diagram (QPI)



5.3. Device Operations

5.3.1. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Error bit, Read Parameter setting (P7-P0) and Wrap Bit Setting (W6-W4).

The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST_R to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

The Enable Reset (66H) command must be issued prior to a Reset(99H) command and any other commands can't be inserted between them. Otherwise, Enable Reset (66H) command will be cleared.

Figure 28. Enable Reset and Reset command Sequence Diagram

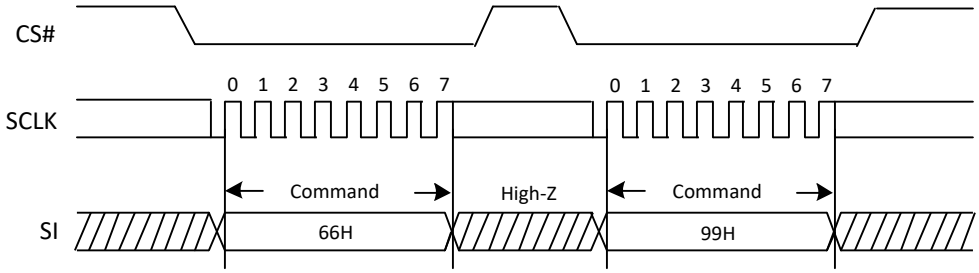
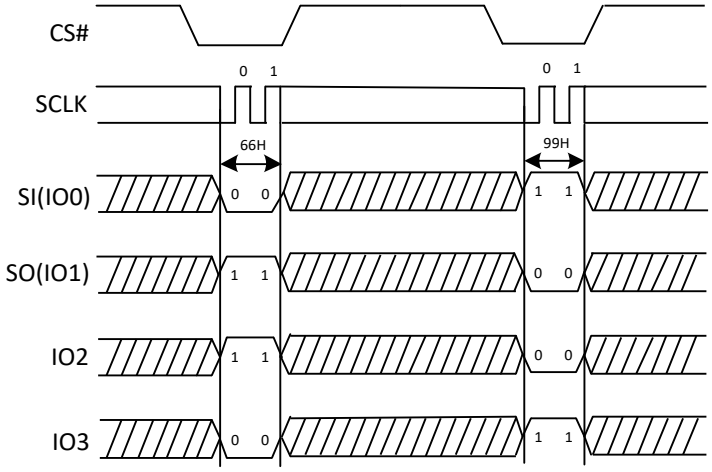


Figure 28a. Enable Reset and Reset command Sequence Diagram (QPI)



5.3.2. Write Enable (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Erase Security Register, Program Security Register and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low → Sending the Write Enable command → CS# goes high.

Figure 29. Write Enable Sequence Diagram

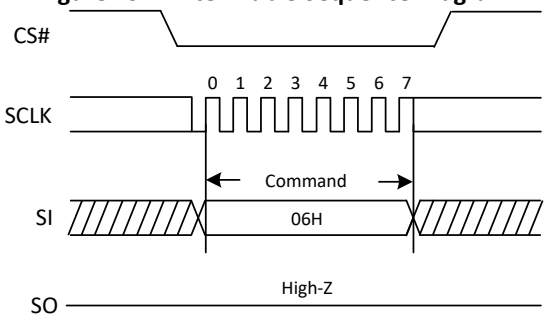
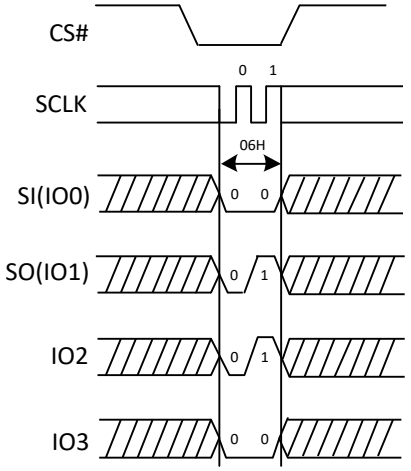


Figure 29a. Write Enable Sequence Diagram (QPI)



5.3.3. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure 30. Write Enable for Volatile Status Register Sequence Diagram

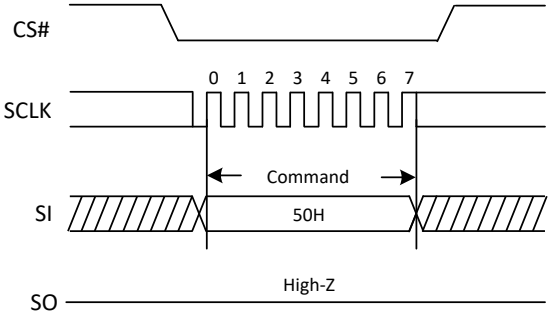
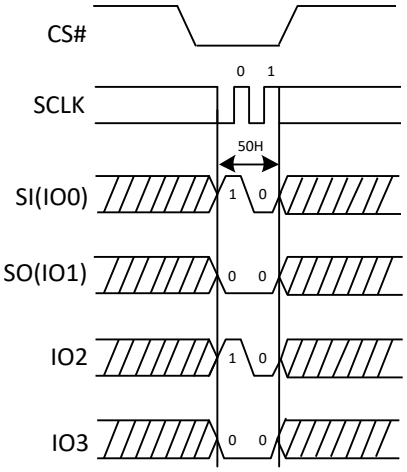


Figure 30a. Write Enable for Volatile Status Register Sequence Diagram (QPI)



5.3.4. Write Disable (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: Write Disable command (WRDI); Power-up; upon completion of the Write Status Register (WRSR), Write Extended Ad-dress Register (WEAR), Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Erase/Program Security Registers and Reset commands.

Figure 31. Write Disable Sequence Diagram

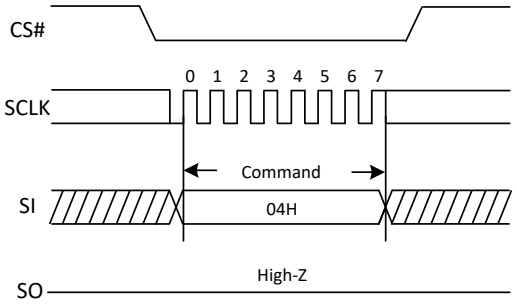
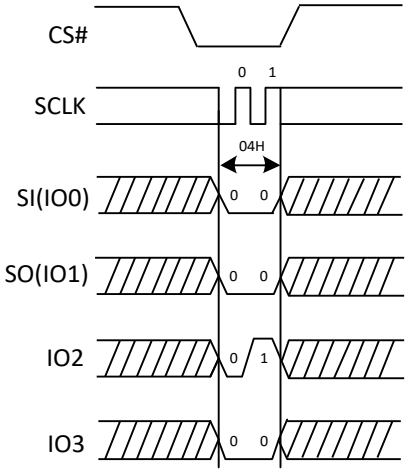


Figure 31a. Write Disable Sequence Diagram (QPI)



5.3.5. Program Erase Suspend (75H)

The Program/Erase Suspend command (75H), allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H, 31H, 11H) and Erase/Program Security Registers command (44H, 42H) and Erase commands (20H, 52H, D8H, C7H, 60H) and Page Program command (02H, 32H) are not allowed during Program suspend. The Write Status Register command (01H, 31H, 11H) and Erase Security Registers command (44H) and Erase commands (20H, 52H, D8H, C7H, 60H) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of "tSUS" (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within "tSUS" and the SUS bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state. The command sequence is shown in figure below.

Figure 32. Program/Erase Suspend Sequence Diagram

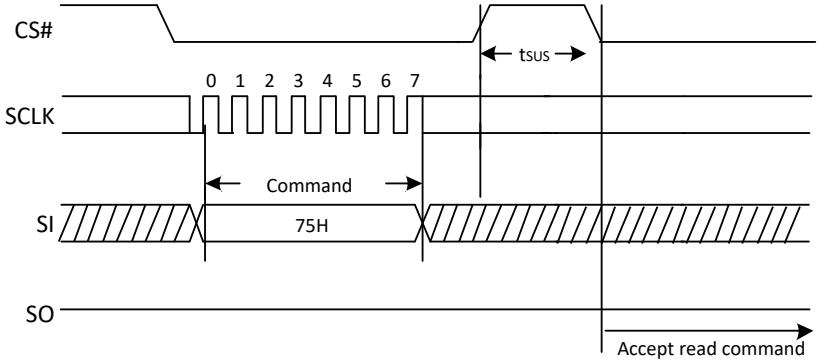
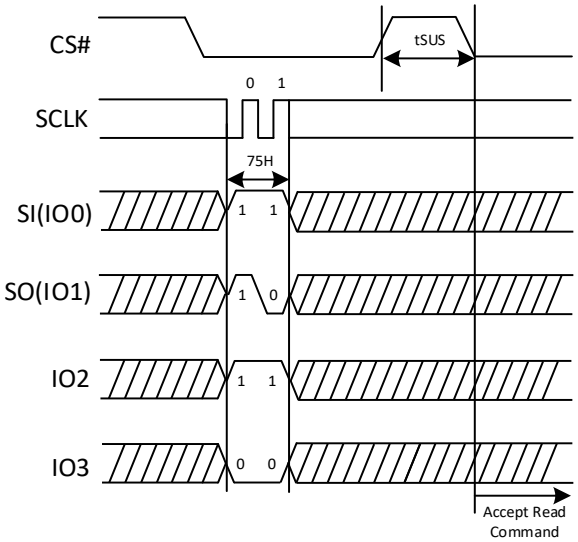


Figure 32a. Program/Erase Suspend Sequence Diagram (QPI)



5.3.6. Program Erase Resume (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase command will be accepted by the device only if the SUS bit equal to 1 and the WIP bit equal to 0. After issued the SUS bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active. The command sequence is shown in the figure below.

Figure 33. Program/Erase Resume Sequence Diagram

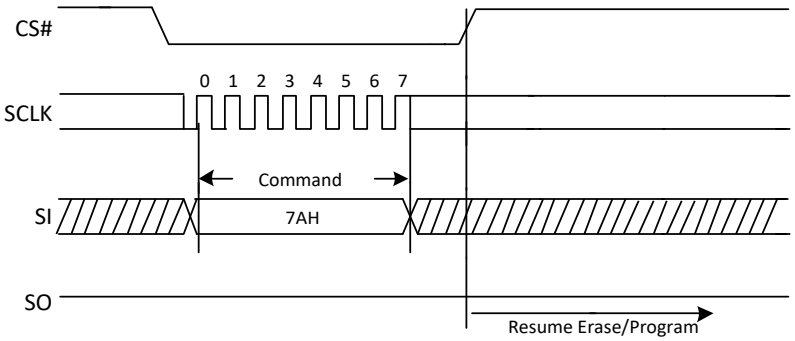
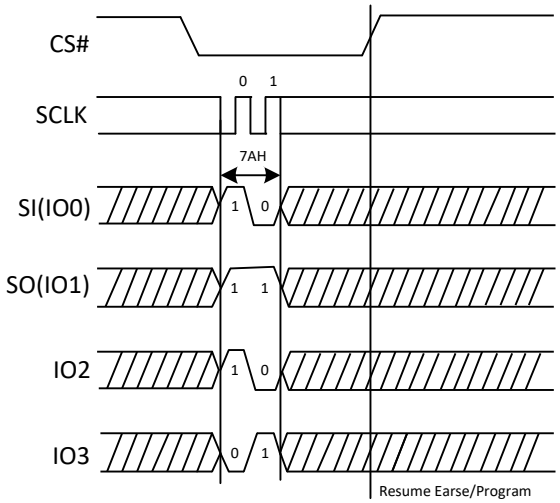


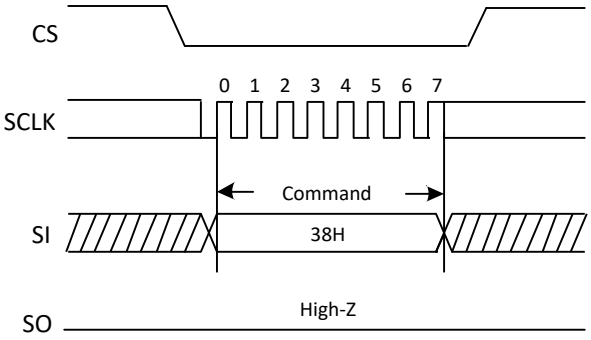
Figure 33a. Program/Erase Resume Sequence Diagram (QPI)



5.3.7. Enable QPI (38H)

The device support both Standard/Dual/Quad SPI and QPI mode. The "Enable QPI (38H)" command can switch the device from SPI mode to QPI mode. See the command Table 2 for all support QPI commands. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged.

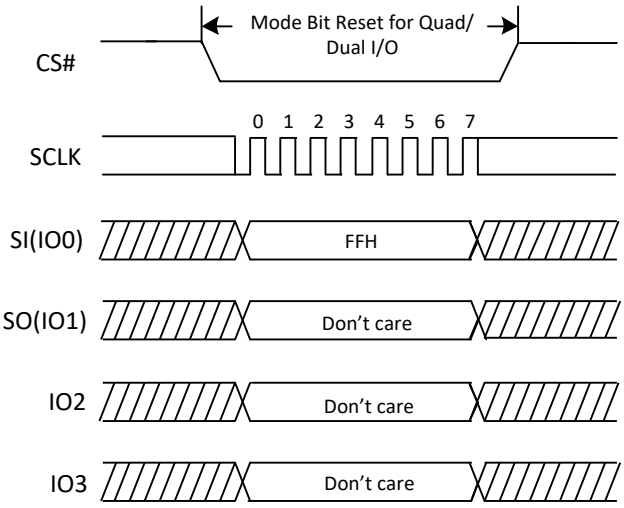
Figure 34. Enable QPI mode command Sequence Diagram



5.3.8. Continuous Read Mode Reset / Disable QPI (FFH)

The Dual/Quad I/O Fast Read operations, "Continuous Read Mode" bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/BCH/EBH/ECH/E7H/BDH/EDH/EEH command code. If Continuous Read Mode bits are set to "AXH", the device will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the "AXH" state and allow standard SPI command to be recognized. The command sequence is shown in the figure below.

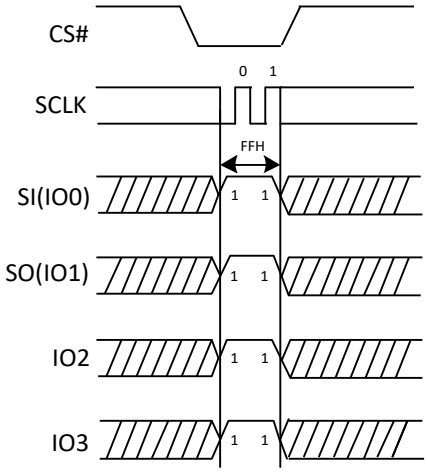
Figure 35. Continuous Read Mode Reset Sequence Diagram



Disable QPI (FFH)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, the “Disable QPI (FFH)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged. When the device is in QPI mode, the first FFH command will exit continuous read mode and the second FFH command will exit QPI mode.

Figure 35a. Disable QPI mode command Sequence Diagram



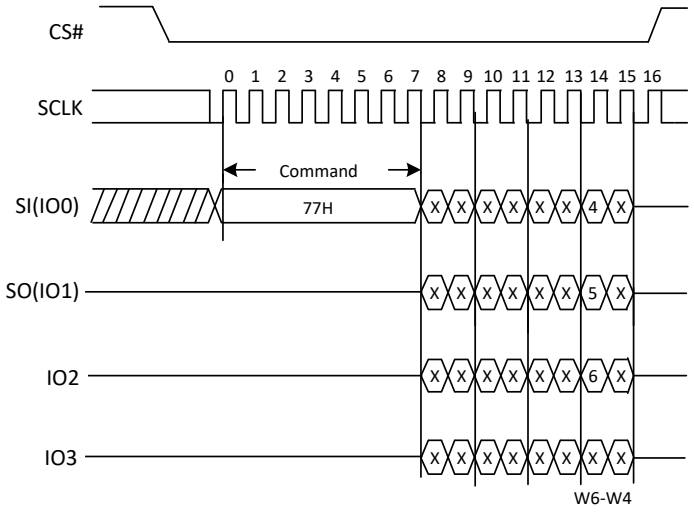
5.3.9. Set Burst With Wrap (77H)

The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read", "Quad I/O Word Fast Read" and "Quad Read Under DTR" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode. The Set Burst with Wrap command sequence: CS# goes low →Send Set Burst with Wrap command →Send 24 dummy bits →Send 8 bits "Wrap bits"→CS# goes high.

W6,W5	W4=0		W4=1(default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0,0	Yes	8-byte	No	N/A
0,1	Yes	16-byte	No	N/A
1,0	Yes	32-byte	No	N/A
1,1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read", "Quad I/O Word Fast Read" and "Quad Read Under DTR" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1. The Wrap Length set by W5-W6 in Standard SPI mode is still valid in QPI mode and can also be re-configured by "Set Read Parameters (C0H) command.

Figure 36. Set Burst with Wrap Sequence Diagram



5.3.10. Set Read Parameters (C0H)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0H)” instruction can be used to configure the number of dummy clocks for “Fast Read (0BH/0CH)”, “Fast Read Quad I/O (EBH/ECH)”, “Read Serial Flash Discoverable Parameters (5AH)” and “Read Unique ID (4BH)” instructions. In Standard SPI mode, the “Set Read Parameters (C0H)” instruction is not accepted.

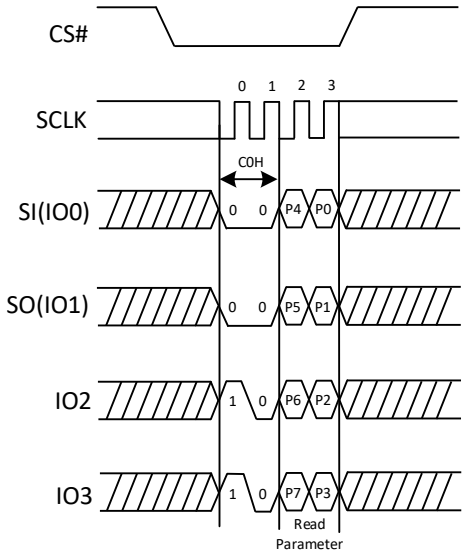
The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed and will remain unchanged when the device is switched from Standard SPI mode to QPI mode and requires to be set again, prior to any 0BH/0CH, EBH/ECH, EDH/EEH instructions. When the device is switched from QPI mode to SPI mode, the number of dummy clocks goes back to default.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 8. The “Wrap Length” is set by W6-4 bit in the “Set Burst with Wrap (77H)” instruction in Standard SPI mode and by P1-P0 in the “Set Read Parameters (C0H)” in the QPI mode. The Wrap Length set by P1-P0 in QPI mode is still valid in SPI mode and can also be re-configured by “Set Burst with Wrap (77H)”.

“C0H” adds an extra bit P2 for Disable/Enable Wrap function. Execute C0H and then follows EBH or ECH, performs the read operation with “Wrap Around” in QPI mode. This function is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command. Also EDH and EEH are alternative ways to perform “Wrap Around” under QPI mode.

P5-P4	Dummy Clocks	Maximum Read Frequency	P2	P1-P0	Wrap Length
0 0	4	64MHz	Enable Wrap=0	0 0 (Default)	8-byte
0 1	4	64MHz	Disable Wrap=1 (Default)	0 1	16-byte
1 0	6	80MHz		1 0	32-byte
1 1 (Default)	8	80MHz		1 1	64-byte

Figure 37. Set Read Parameters command Sequence Diagram



5.3.11. Enable 4-byte Mode (B7H)

The Enable 4-byte Mode command enables accessing the address length of 32-bit for the memory area of the higher density (larger than 128Mb). The device default is in 24-bit address mode. After sending the Enable 4-byte Mode command, the ADS bit will be set to 1 to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24 bit. The Disable 4-byte mode or Reset or Power-off will disable 4-byte mode.

Figure 38. Enable 4-byte Mode Sequence Diagram (SPI)

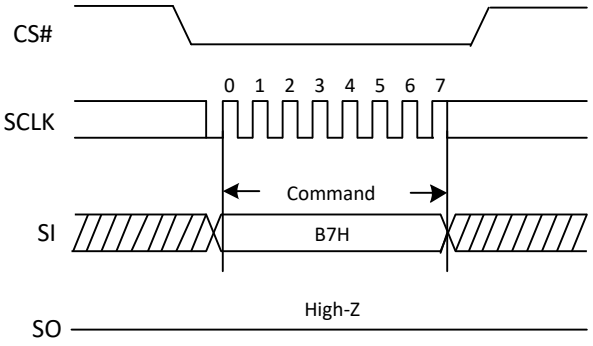
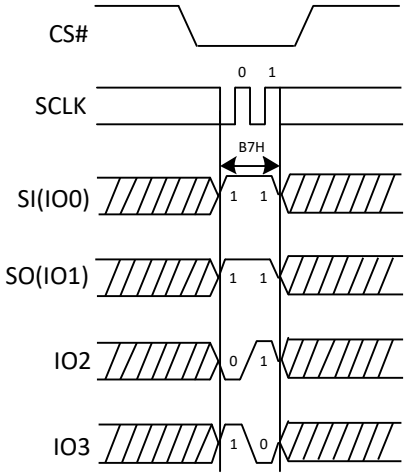


Figure 38a. Enable 4-byte Mode Sequence Diagram (QPI)



5.3.12. Disable 4-byte Mode (E9H)

The Disable 4-byte Mode command is executed to exit the 4-byte address mode and return to the default 3-byte address mode. After sending the Disable 4-byte Mode command, the ADS bit will be clear to be 0 to indicate the 4-byte address mode has been disabled, and then the address length will return to 24-bit.

Figure 39. Disable 4-byte Mode Sequence Diagram (SPI)

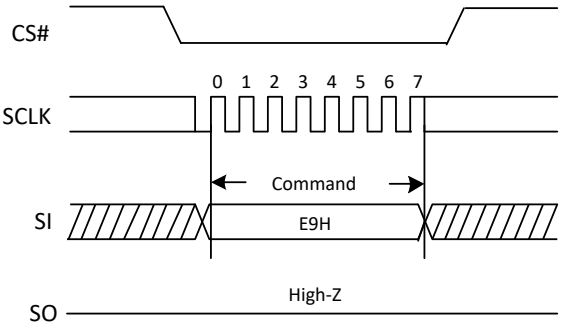
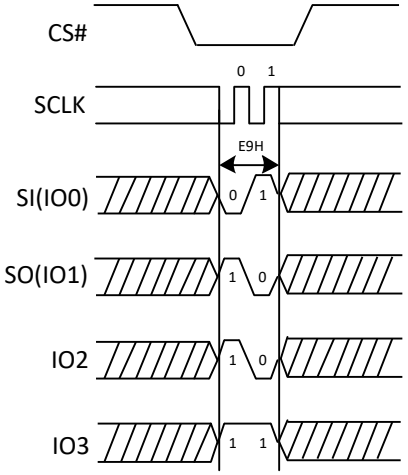


Figure 39a. Disable 4-byte Mode Sequence Diagram (QPI)



5.3.13. Clear SR Flags (30H)

The Clear Status Register Flags command resets S18 (Program Error bit) and S19 (Erase Error bit) from status register. It is not necessary to set the WEL bit before the Clear Status Register command is executed. The Clear SR command will be not accepted even when the device remains busy with WIP set to 1, as the device does remain busy when either error bit is set. The WEL bit will be unchanged after this command is executed.

Figure 40. Clear Status Register Flags Sequence Diagram (SPI)

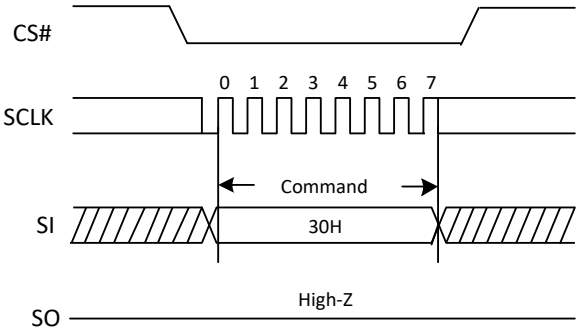
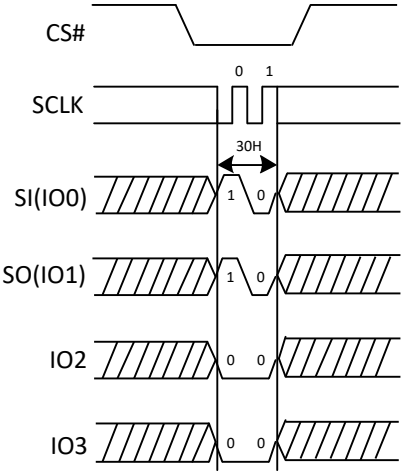


Figure 40a. Clear Status Register Flags Sequence Diagram (QPI)



5.3.14. Deep Power Down (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest power consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But the Standby Mode is different from the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the flash memory has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command(ABH) and Software Reset(66H + 99H). These commands release the device from the Deep Power-Down Mode.

The Deep Power-Down Mode automatically stops at Power-Off, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI, driving CS# high.

The Deep Power-Down command sequence: CS# goes low→sending Deep Power-Down command→CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command will not be executed. As soon as CS# is driven high, it requires a time duration of tDP before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any input of Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 41. Deep Power-Down Sequence Diagram

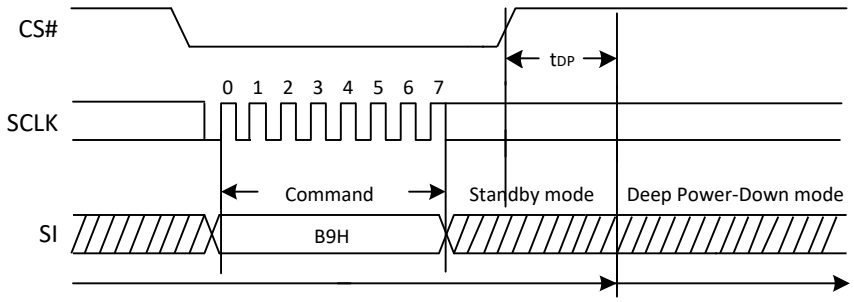
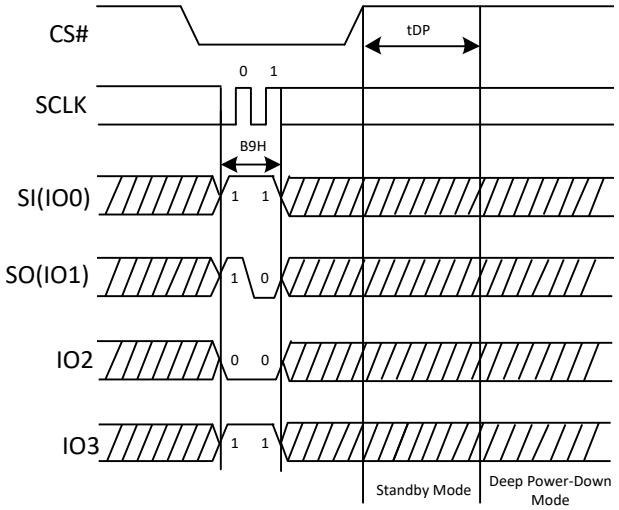


Figure 41a. Deep Power-Down Sequence Diagram (QPI)



5.3.15. Release From Deep Power Down (ABH)

The Release from Deep Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from Deep Power-Down Mode or obtain the devices electronic identification (ID) number.

To release the device from Deep Power-Down Mode, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown in Figure 42. Release from Deep Power-Down Mode will take the time duration of tRES1 (See AC Characteristics) before the device resume to normal state and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When the command is used only to obtain the Device ID while the flash memory is not in Deep Power-Down Mode, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 42b. The Device ID value for the device is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When the command is used to release the device from Deep Power-Down Mode and obtain the Device ID, the command is the same as previously described, and shown in Figure 42b. except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume to normal mode and other command will be accepted. If the Release from Deep Power-Down and Read Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command will be ignored and will not affect the current cycle.

Figure 42. Release Power-Down Sequence Diagram

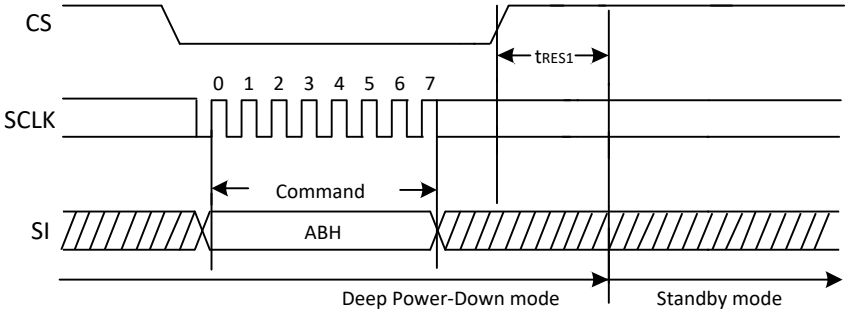


Figure 42a. Release Power-Down Sequence Diagram (QPI)

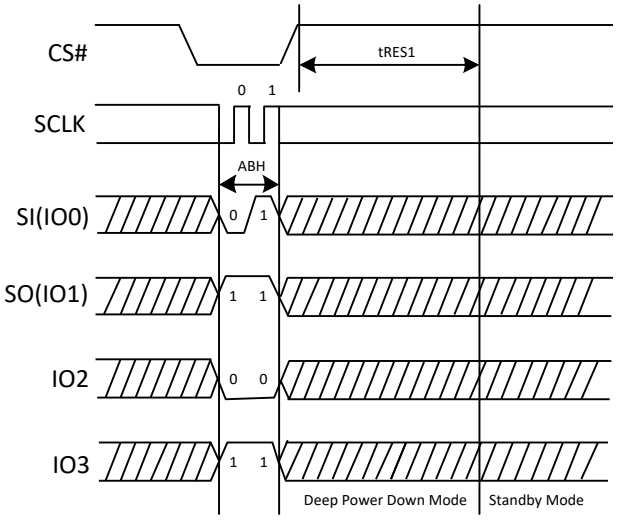


Figure 42b. Release Power-Down/Read Device ID Sequence Diagram

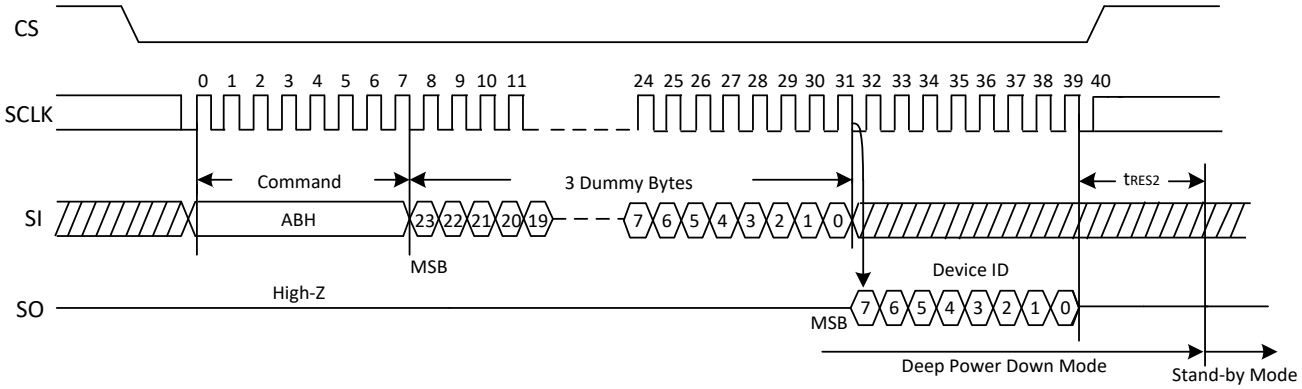
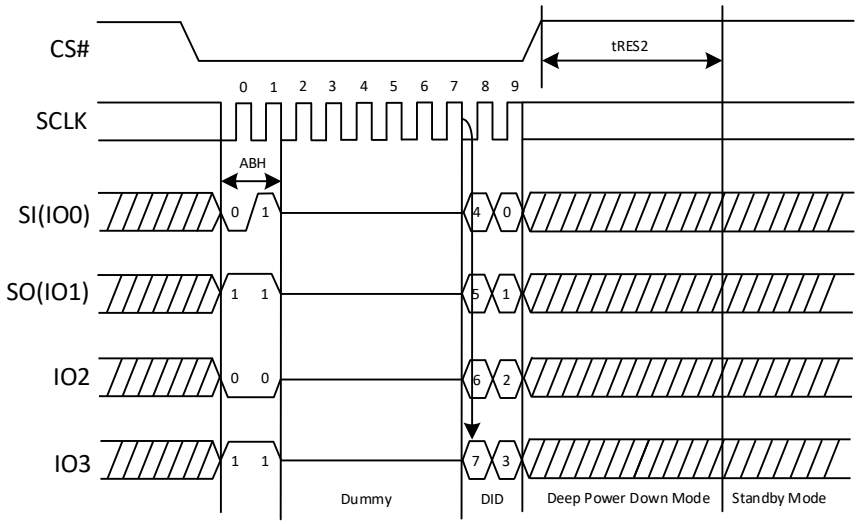


Figure 42c. Release Power-Down/Read Device ID Sequence Diagram (QPI)



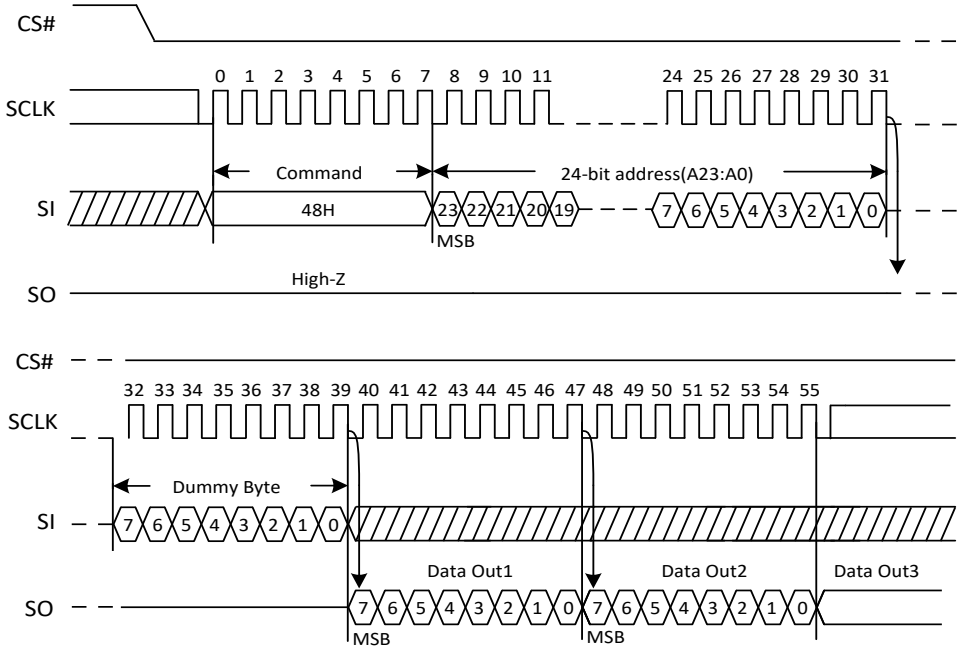
5.4. One-Time Programmable (OTP) Operations

5.4.1. Read Security Register (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

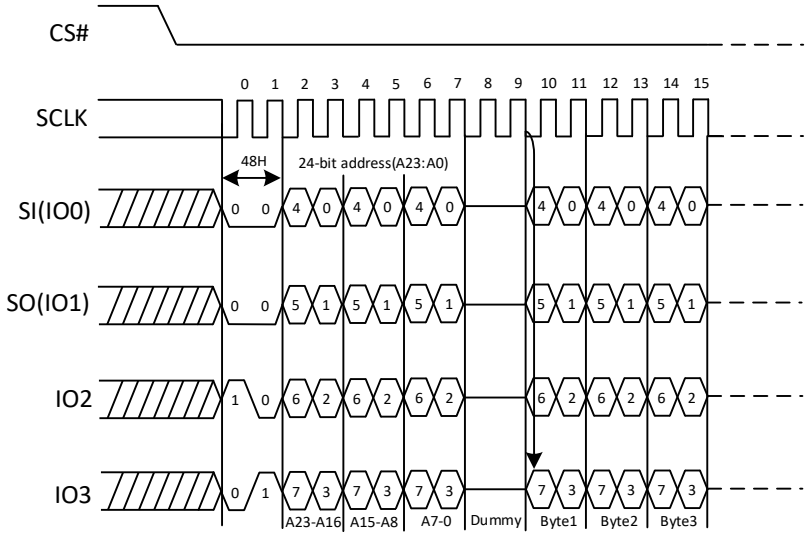
ADDRESS	A23-A14	A13-A12	A11-A10	A9-A0
Security Register 1	don't care	01b	00b	Byte Address
Security Register 2	don't care	10b	00b	Byte Address

Figure 43. Read Security Registers command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 43a. Read Security Registers command Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

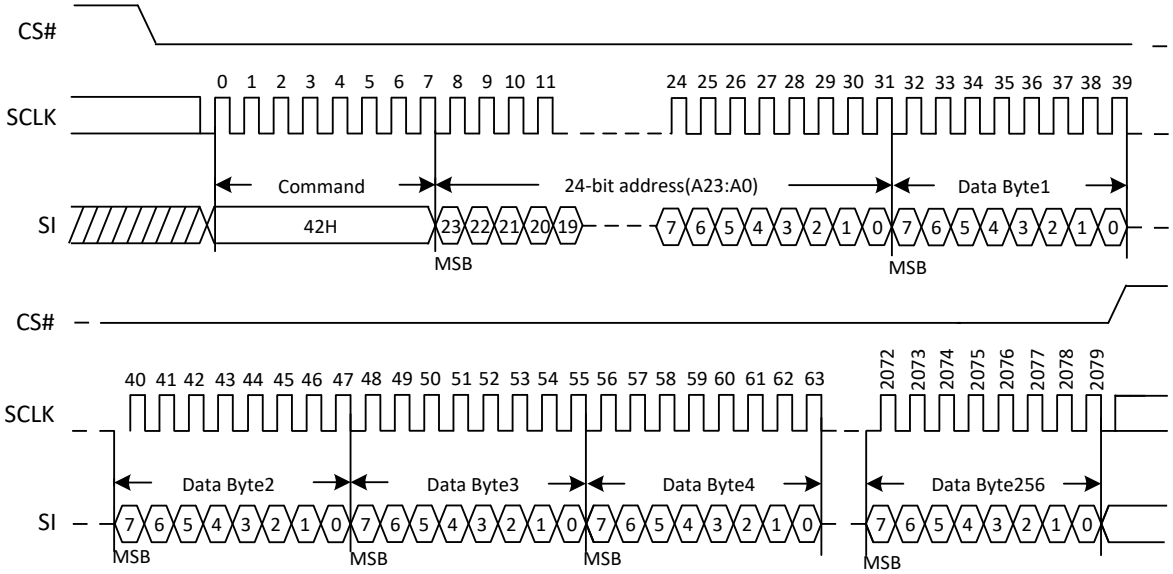
5.4.2. Program Security Register (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB1) is set to 1, the Security Registers 1 will be permanently locked. If the Security Registers Lock Bit (LB2) is set to 1, the Security Registers 2 will be permanently locked. Program Security Registers command will be ignored.

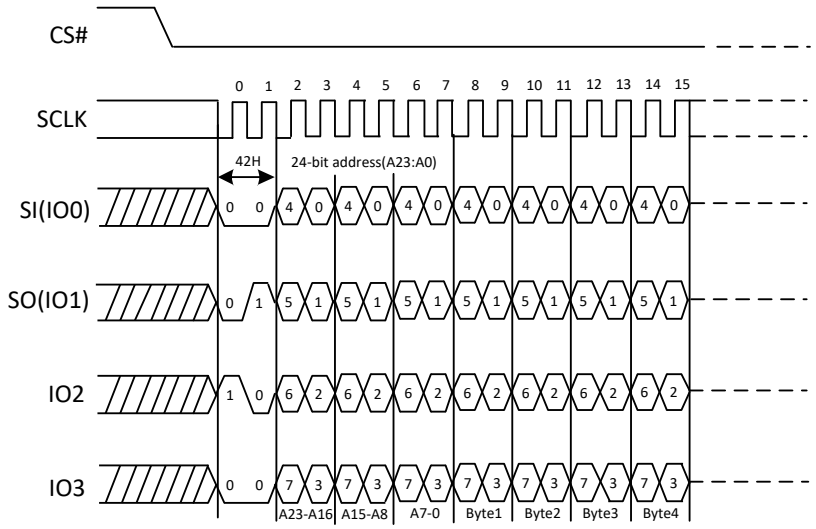
ADDRESS	A23-A14	A13-A12	A11-A10	A9-A0
Security Register 1	don't care	01b	00b	Byte Address
Security Register 2	don't care	10b	00b	Byte Address

Figure 44. Program Security Registers command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 44a. Program Security Registers command Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.4.3. Erase Security Register (44H)

The device provides two 1024-byte Security Registers which only erased each 1024-byte at once. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

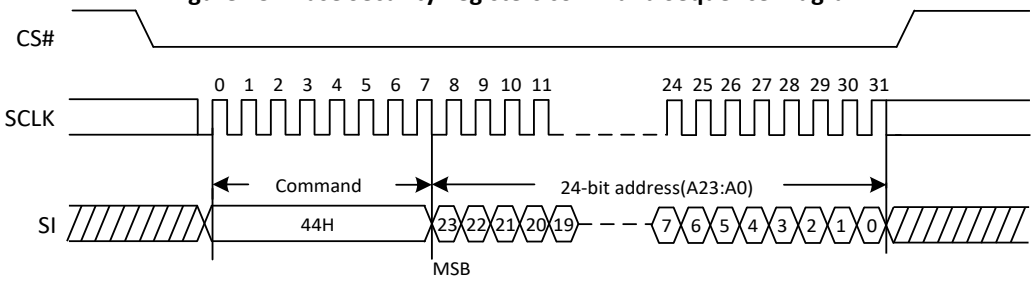
The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low→sending Erase Security Registers Command →sending 3-byte address or 4-byte address on SI→CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Security Registers Lock Bit (LB1, LB2) in the Status Register can be used to OTP protect the security registers. If the Security Registers Lock Bit (LB1) is set to 1, the Security Registers 1 will be permanently locked; If the Security Registers Lock Bit (LB2) is set to 1, the Security Registers 2 will be permanently locked, the Erase Security Registers command will be ignored.

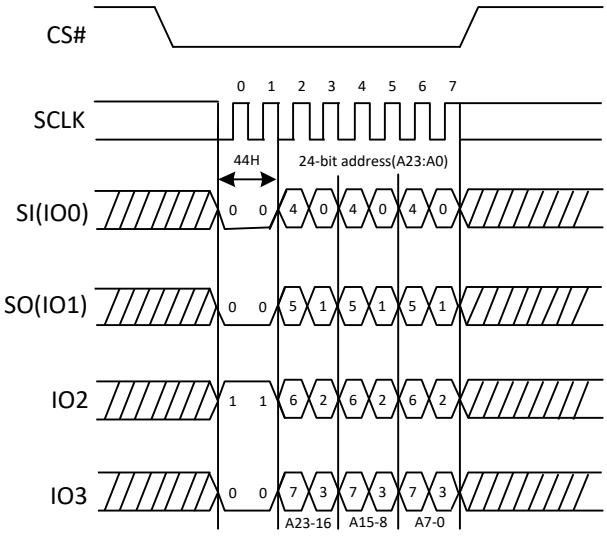
ADDRESS	A23-A14	A13-A12	A11-A10	A9-A0
Security Register1	don't care	01b	00b	don't care
Security Register2	don't care	10b	00b	don't care

Figure 45. Erase Security Registers command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 45a. Erase Security Registers command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

5.5. Advanced Sector Protection Operations

5.5.1. Global Block/Sector Lock (7EH) or Unlock (98H)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock command, or can set to 0 by the Global Block/Sector Unlock command.

The Global Block/Sector Lock command (7EH) sequence: CS# goes low → SI: Sending Global Block/Sector Lock command → CS# goes high. The command sequence is shown in Figure 46.

The Global Block/Sector Unlock command (98H) sequence: CS# goes low → SI: Sending Global Block/Sector Unlock command → CS# goes high. The command sequence is shown in Figure 46b.

Figure 46. The Global Block/Sector Lock Sequence Diagram

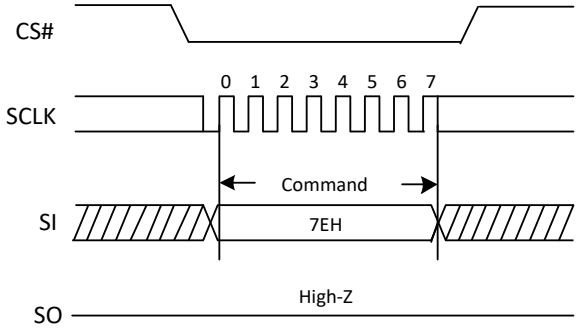


Figure 46a. The Global Block/Sector Lock Sequence Diagram (QPI)

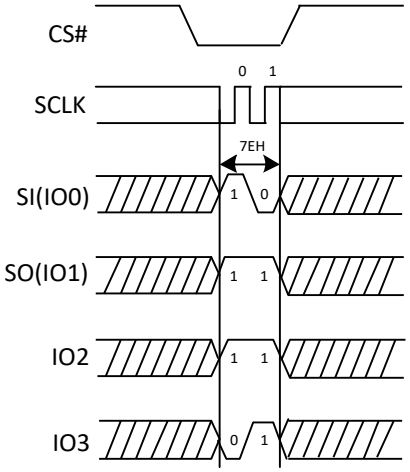


Figure 46b. The Global Block/Sector Unlock Sequence Diagram

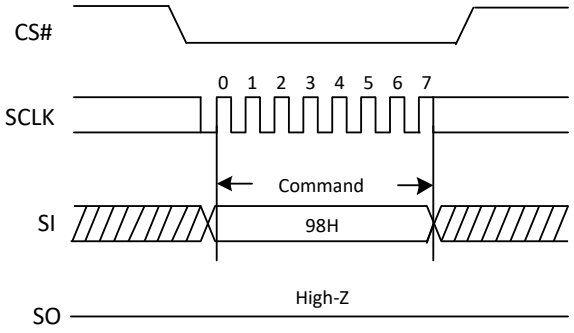
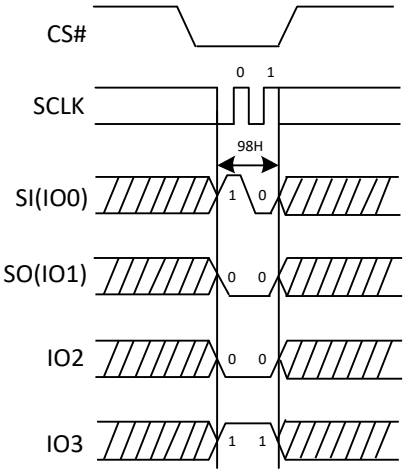


Figure 46c. The Global Block/Sector Unlock Sequence Diagram (QPI)



5.5.2. Individual Block/Sector Lock (36H)/Unlock (39H)/Read (3DH)

The individual block/sector lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, T/B, BP (3:0) bits in the Status Register. The Individual Block/Sector Lock bits are volatile bits, the default values of which after device power up or after a Reset are 1.

The individual Block/Sector Lock command (36H) sequence: CS# goes low → SI: Sending individual Block/Sector Lock command → SI: Sending 3-byte address or 4-byte address individual Block/Sector Lock Address → CS# goes high. The command sequence is shown in Figure 47.

The individual Block/Sector Unlock command (39H) sequence: CS# goes low → SI: Sending individual Block/Sector Unlock command → SI: Sending 3-byte address or 4-byte address individual Block/Sector Lock Address → CS# goes high. The command sequence is shown in Figure 47b.

The Read individual Block/Sector lock command (3DH) sequence: CS# goes low → SI: Sending Read individual Block/Sector Lock command → SI: Sending 3-byte address or 4-byte address individual Block/Sector Lock Address → SO: The Block/Sector Lock Bit will out → CS# goes high. If the least significant bit(LSB) is 1, the corresponding block/sector is locked, if the LSB is 0, the corresponding block/sector is unlocked, Erase/Program operation can be performed. The command sequence is shown in Figure 47d.

Figure 47. Individual Block/Sector Lock command Sequence Diagram

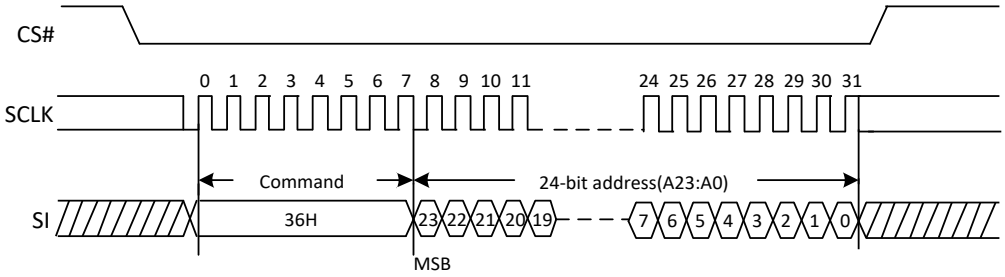


Figure 47a. Individual Block/Sector Lock command Sequence Diagram (QPI)

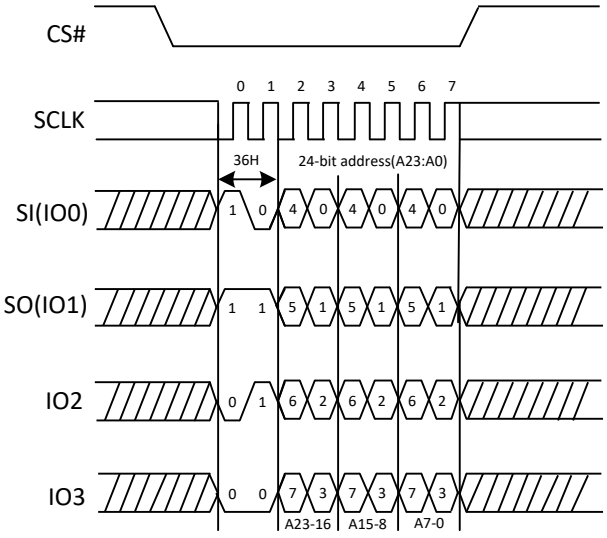


Figure 47b. Individual Block/Sector Unlock command Sequence Diagram

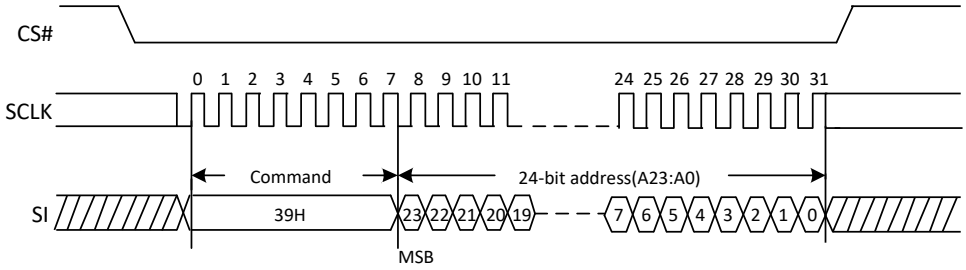


Figure 47c. Individual Block/Sector Unlock command Sequence Diagram (QPI)

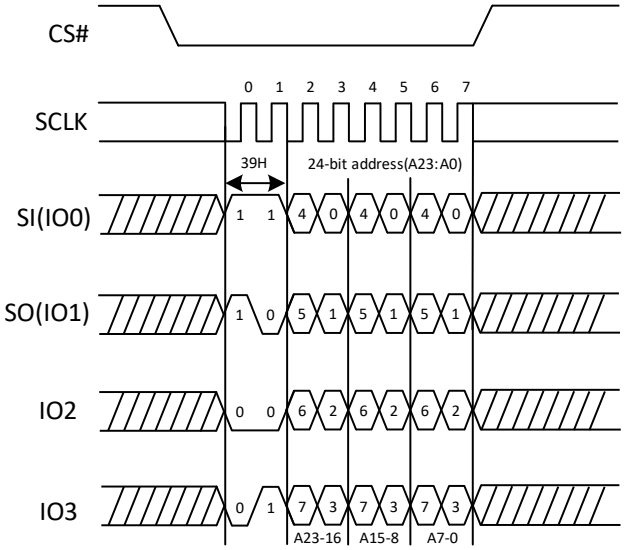


Figure 47d. Read Individual Block/Sector lock command Sequence Diagram

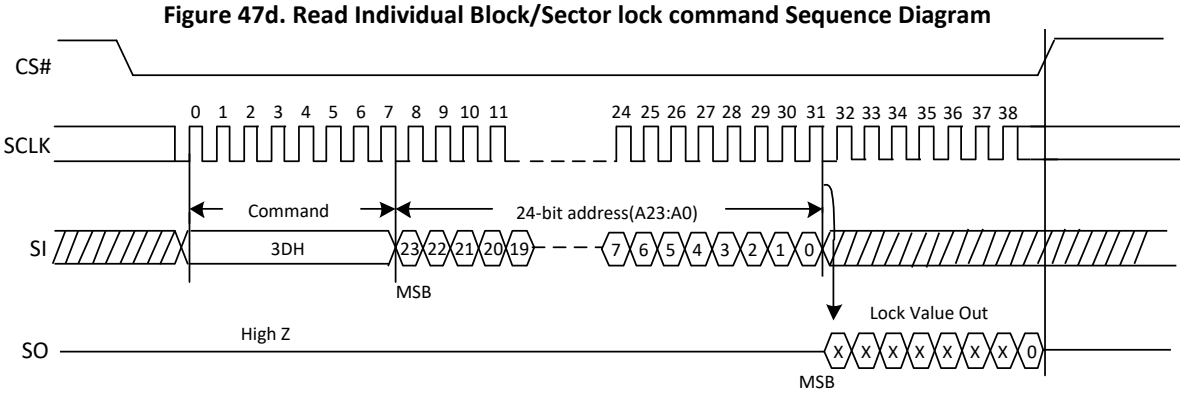
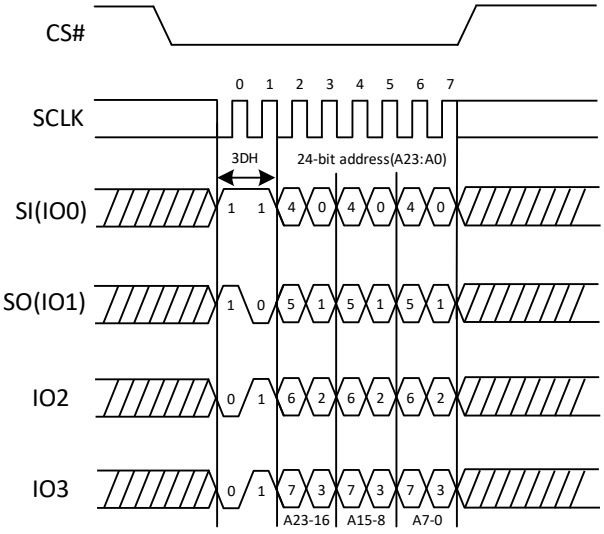
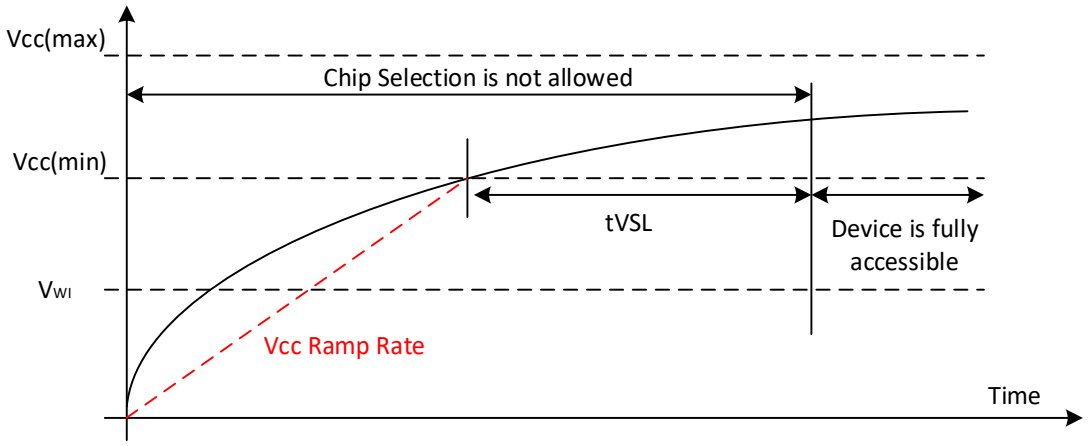


Figure 47e. Read Individual Block/Sector lock command Sequence Diagram (QPI)



6. ELECTRICAL CHARACTERISTICS

6.1. Power-on Timing



Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min) To CS# Low	1	-	ms
VWI	Write Inhibit Voltage	1	1.5	V
	VCC Ramp Rate	2	-	V/ms

Note：VCC ramp rate must exceed 2V/ms otherwise a Hardware reset would be required.

6.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH). All Status Register bits except S22 bits are 0, S22 bit is 1.

6.3. Data Retention and Endurance

Parameter	Typ.	Unit
Data Retention Time	20	Years
Erase/Program Endurance	100K	Cycles

6.4. Latch up Characteristics

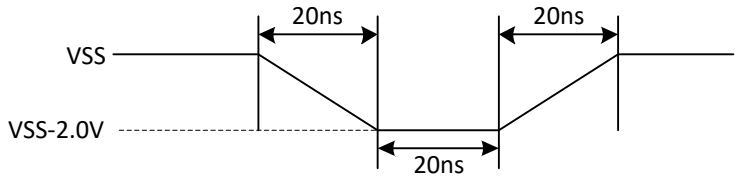
Parameter	Min.	Max.
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-200mA	200mA

6.5. Absolute Maximum Ratings

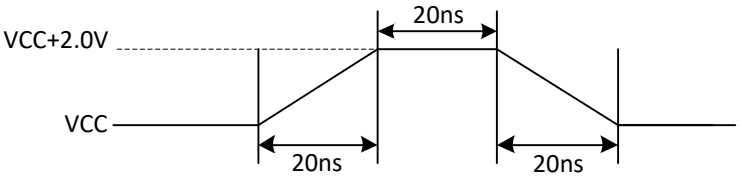
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	°C
Storage Temperature	-65 to 150	°C
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



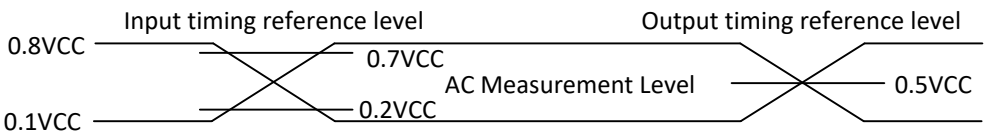
Maximum Positive Overshoot Waveform



6.6. Capacitance Measurement Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage		0.5VCC		V	

Absolute Maximum Ratings Diagram



Note：Input pulse rise and fall time are <5ns

6.7. DC Characteristics

(TA=-40°C~85°C, VCC=2.70~3.60V)

Symbol	Parameter	Test Condition	Min.	Typ.(1)	Max.	Unit
ILI	Input Leakage Current				±2	µA
ILO	Output Leakage Current				±2	µA
ICC1	Standby Current	CS#=VCC VIN=VCC or VSS		15	90	µA
ICC2	Deep Power-Down Current	CS#=VCC VIN=VCC or VSS		0.5	10	µA
ICC3 Note3	Operating Current (Read)	CLK=0.1VCC/0.9VCC at 108MHz, Q=Open (*1,*2,*4 I/O)		10	30	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open (*1,*2,*4 I/O)		8	22	mA
		CLK=0.1VCC/0.9VCC at 48MHz, Q=Open (*1,*2,*4 I/O)		6	17	mA
ICC4	Operating Current (PP)	CS#=VCC			40	mA
ICC5	Operating Current (WRSR)	CS#=VCC			10	mA
ICC6	Operating Current (SE)	CS#=VCC			40	mA
ICC7	Operating Current (BE)	CS#=VCC			40	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.7VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL=1.6mA			0.4	V
VOH	Output High Voltage	IOH=-100µA	VCC-0.2			V

Note:
1. Typical values given for TA=25°C, VCC=3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Typical values of ICC3 given for Pattern 00 FF.

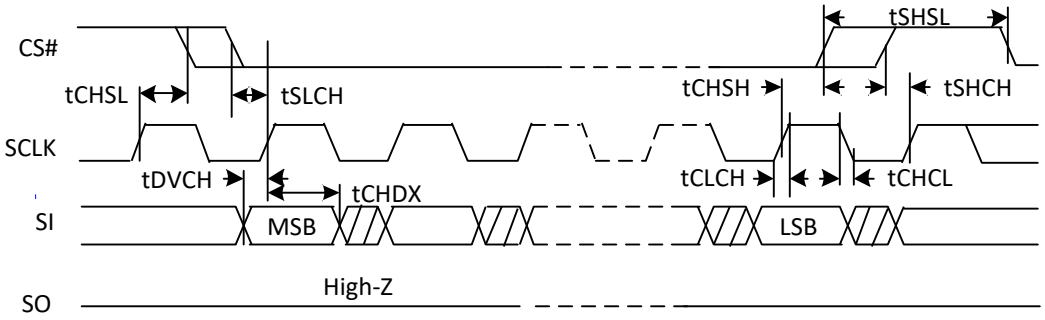
6.8. AC Characteristics

(TA=-40°C~85°C, VCC=2.7~3.6V, CL=30pF)

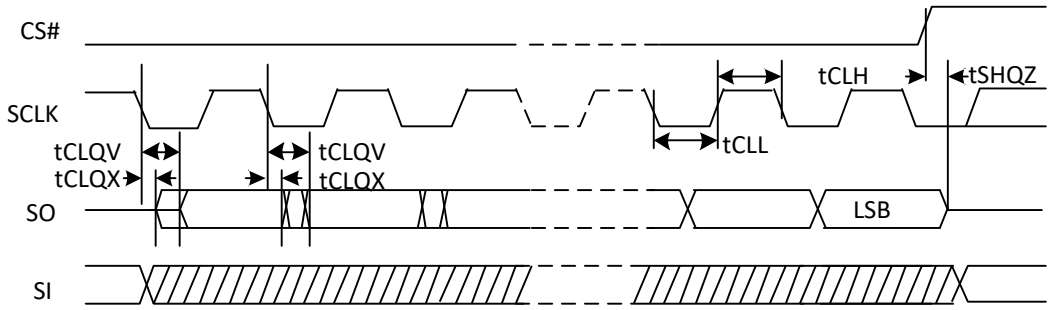
Symbol	Parameter	Min.	Typ.(2)	Max.	Unit
fC1(3)	Serial Clock Frequency For: All command except for 03H, 3BH, BBH, 6BH, EBH, E7H, 94H under SPI Mode, QPI and DTR instructions	D.C.		120	MHz
fC2(3)	Serial Clock Frequency For 3BH, 6BH	D.C.		108	MHz
fC3(3)	Serial Clock Frequency For BBH, EBH, E7H, 94H	D.C.		104	MHz
fC4(3)	Clock frequency QPI instructions	D.C.		80	MHz
fC5(3)	Clock frequency DTR instructions	D.C.		50	MHz
fR	Serial Clock Frequency For: Read Data(03H)	D.C.		80	MHz
tCLH(1)	Serial Clock High Time	45%PC			ns
tCLL(1)	Serial Clock Low Time	45%PC			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	3			ns
tSHCH	CS# Not Active Setup Time	3			ns
tCHSL	CS# Not Active Hold Time	3			ns
tSHSL	CS# High Time (read/write)	20			ns
tSHQZ	Output Disable Time			9	ns
tCLQX	Output Hold Time	2			ns
tCLQV	Clock Low To Output Valid			8	ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tDP	CS# High To Deep Power-Down Mode			7	µs
tRES1	CS# High To Standby Mode Without Electronic Signature Read			7	µs
tRES2	CS# High To Standby Mode With Electronic Signature Read			7	µs
tRST_R	CS# High To Next Command After Reset (from read)			20	µs
tRST_P	CS# High To Next Command After Reset (from program)			20	µs
tRST_E	CS# High To Next Command After Reset (from erase)			20	µs
tSUS	CS# High To Next Command After Suspend			50	µs
tRS	Latency Between Resume And Next Suspend	400			µs
tW	Write Status Register Cycle Time		1	20	ms
tPP	Page Programming Time		0.25	1.25	ms
tBP	Byte Programming Time (First Byte)		30	100	µs
tSE	Sector Erase Time		40	1500	ms
tBE1	Block Erase Time (32K Bytes)		0.15	4	s
tBE2	Block Erase Time (64K Bytes)		0.22	5	s
tCE	Chip Erase Time		70	300	s

Note:
1. Clock high or Clock low must be more than or equal to 45%PC. PC=1/fC(MAX).
2. Typical values given for TA=25°C, VCC=3.3V. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Maximum Serial Clock Frequencies are measured results picked at the falling edge.

Serial Input Timing

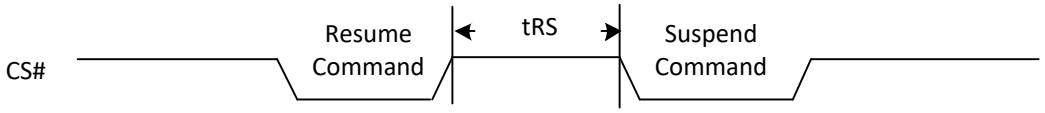


Output Timing



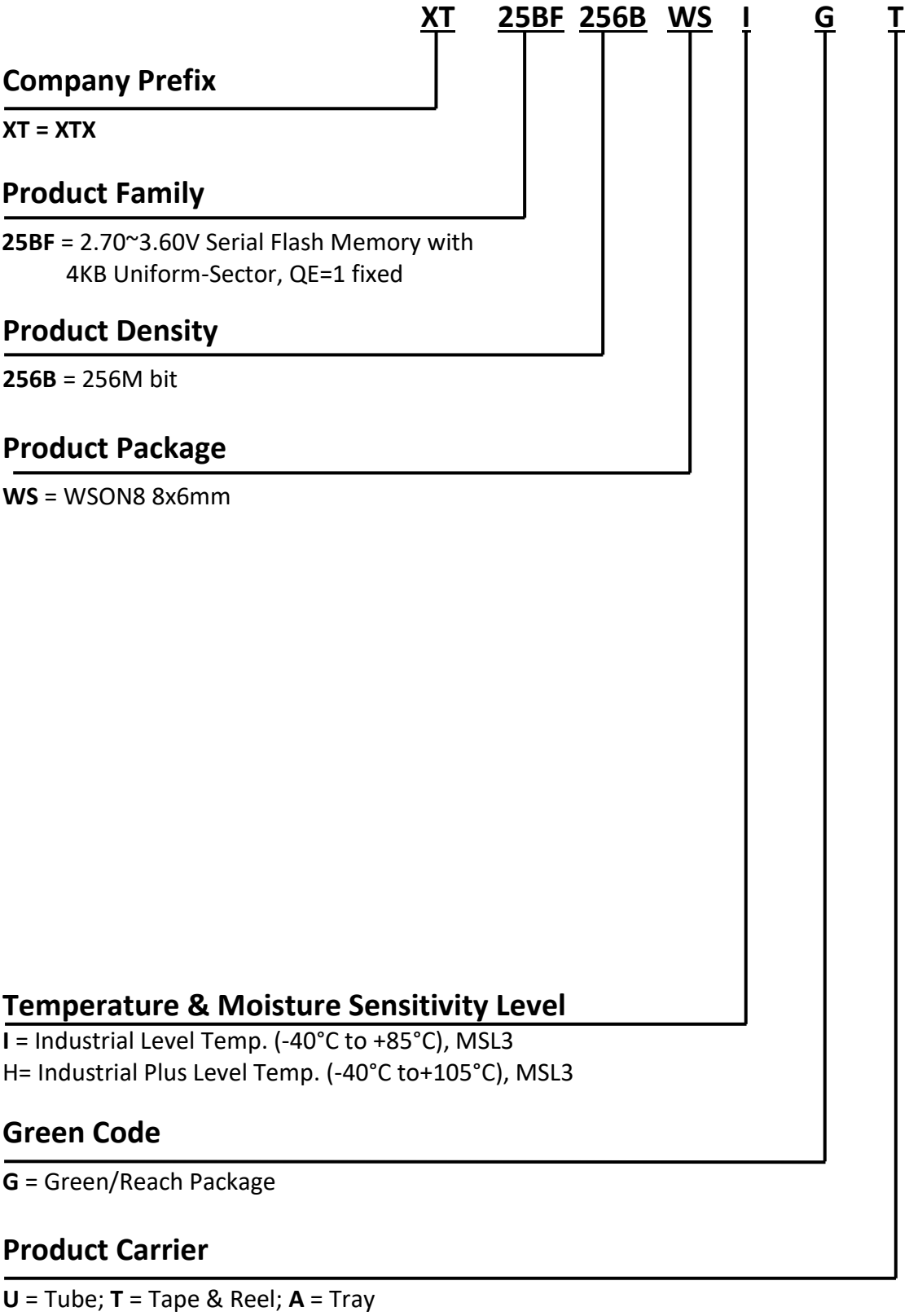
Least significant address bit (LSB) in

Resume to Suspend Timing Diagram



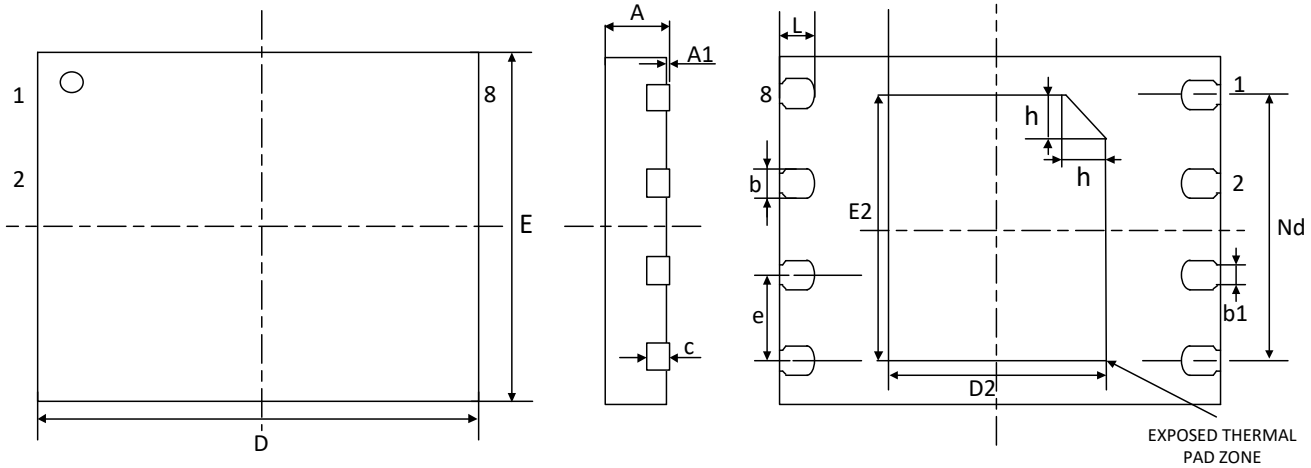
7. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following

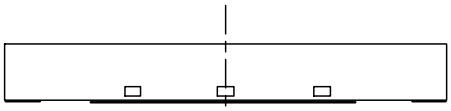


8. PACKAGE INFORMATION

8.1. Package WSON8 8x6mm



TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
b1		0.25REF	
c	0.18	0.20	0.25
D	7.90	8.00	8.10
Nd		3.81BSC	
e		1.27BSC	
E	5.90	6.00	6.10
D2	3.30	3.40	3.50
E2	4.20	4.30	4.40
L	0.45	0.50	0.55
h	0.30	0.35	0.40

9. REVISION HISTORY

Revision	Description	Date
1.0	Initial version	Nov-26-2020
1.1	Changed 92H/94H description and diagram to 4/6 dummy clocks	Dec-9-2020
1.2	Revised to correct Package WSON8 dimensions based on POD	Mar-24-2021
1.3	Revised to change company name and logo Revised to correct Package WSON8 dimensions based on POD	Mar-29-2021
1.4	Update SFDP Table	Apr-23-2021
1.5	Reserved SRP bit Add Absolute Maximum Ratings Diagram Add Note 3 for AC Characteristics	Jul-13-2021
1.6	Adjusted ICC1 max from 50μA to 70μA fC4 max from 80MHz to 50MHz tSHQZ max from 9ns to 14ns tCLQV max from 7ns to 9ns tSUS max from 20μs to 50μs tRS min from 120μs to 400μs the typical of tBP from 20μs to 30μs, max from 30μs to 100μs the typical of tSE from 40ms to 65ms, max from 400ms to 1500ms the typical of tBE1 from 0.15s to 0.38s, max from 1s to 4s the typical of tBE2 from 0.22s to 0.52s, max from 1.5s to 5s Adjusted the description of 4BH Command: 4 Dummy Bytes → 24-bit address (A23:A0) (Don't care) + 1 dummy Byte Update 0BH/OCH(QPI), EBH/ECH(QPI), ABH(QPI),5AH(QPI) / 4BH(QPI) /75H Diagram Deleted SFDP Table,Note: For SFDP Table, please contacted with XTX	Nov 01, 2021
1.7	Updated "Table 2. Commands" Corrected the address length of the command sent in 4-byte mode for 5AH / 90H / 92H / 94H are both 3bytes Adjusted the speed of C0H command with different number of dummy: 4 dummy is 64MHz, 6/8 dummy is 80MHz Added parameter requirements for VCC Ramp Rate in Power-on Timing Adjusted ICC1 max from 70μA to 90μA ICC2 typical from 1μA to 0.5μA ICC2 max from 20μA to 10μA ICC4 max from 30mA to 40mA ICC6 / ICC7 max from 25mA to 40mA QPI frequency max from 96MHz to 80MHz BBH / EBH frequency max from 108MHz to 104MHz E7H / 94H frequency max from 108MHz to 104MHz tSLCH min from 3ns to 5ns tSHQZ max from 14ns to 9ns tCLQV max from 9ns to 8ns	Mar 28, 2022

	tPP Max from 0.75ms to 1.25ms the typical of tSE from 65ms to 40ms the typical of tBE1 from 0.38s to 0.15s the typical of tBE2 from 0.52s to 0.22s	