XT25Q64D

Quad IO Serial NOR Flash
Datasheet

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Serial NOR Flash Memory

1.8V Multi I/O with 4KB, 32KB & 64KB Sector/Block Erase

- **64M -bit Serial Flash**
  - 8192K-byte
  - 256 bytes per programmable page
- **Standard, Dual, Quad SPI, DTR**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#/RESET#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#/RESET#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - QPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - SPI/QPI DTR(Double Transfer Rate) Read
- **Flexible Architecture**
  - Sector of 4K-bytes
  - Block of 32/64k-bytes
- **Advanced security Features**
  - 3*1024-Bytes Security Registers With OTP Lock
- **Support 128 bits Unique ID**
- **Software/Hardware Write Protection**
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top or Bottom, Sector or Block selection
- **Continuous Read With 8/16/32/64-byte Wrap**
- **Erase/Program Suspend/Resume**
- **Package Options**
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- **Temperature Range & Moisture Sensitivity Level**
  - Industrial Level Temperature. (-40℃ to +85℃), MSL3
- **Low Power Consumption**
  - 0.4uA typical Power-Down current
- **Single Power Supply Voltage**
  - 1.65~2.0V
- **Endurance and Data Retention**
  - Minimum 100,000 Program/Erase Cycle
  - 20-year Data Retention typical
- **High Speed Clock Frequency**
  - 133MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 266Mbits/s
  - Quad I/O Data transfer up to 532Mbits/s
  - QPI Mode Data transfer up to 432Mbits/s
  - DTR Quad I/O Data transfer up to 768Mbits/s
- **Program/Erase Speed**
  - Page Program time: 0.4ms typical
  - Sector Erase time: 40ms typical
  - Block Erase time: 0.12/0.15s typical
  - Chip Erase time: 20s typical

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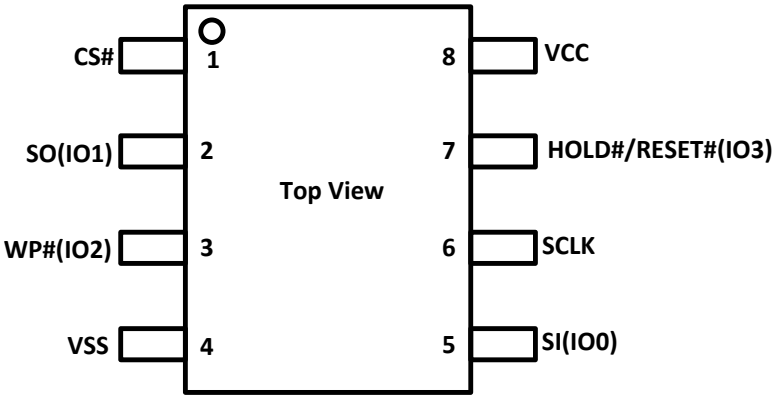
1. GENERAL DESCRIPTION

The XT25Q64D (64M-bit) Serial flash supports standard Serial Peripheral Interface (SPI), Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#/RESET#).

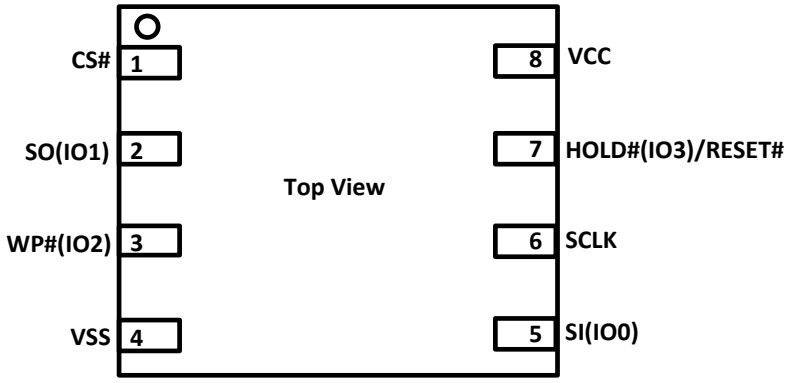
1.1. Available Ordering OPN

OPN	Package Type	Package Carrier
XT25Q64DSSIGU	SOP8 208mil	Tube
XT25Q64DSSIGT	SOP8 208mil	Tape & Reel
XT25Q64DWOIGT	WSON8 6x5mm	Tape & Reel
XT25Q64DWLIGT	WLCSP-WL	Tape & Reel
XT25Q64DLCIGT	WLCSP-LC	Tape & Reel

1.2. Connection Diagram

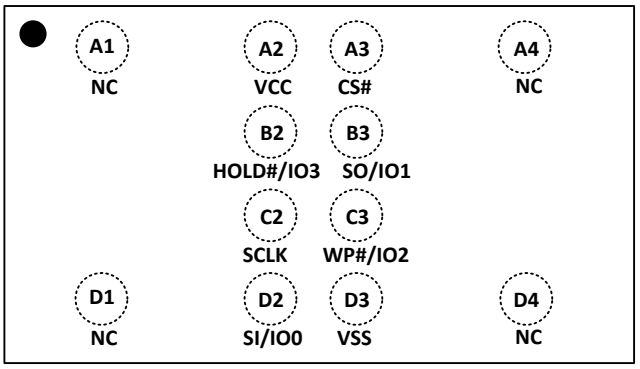


8-pin SOP

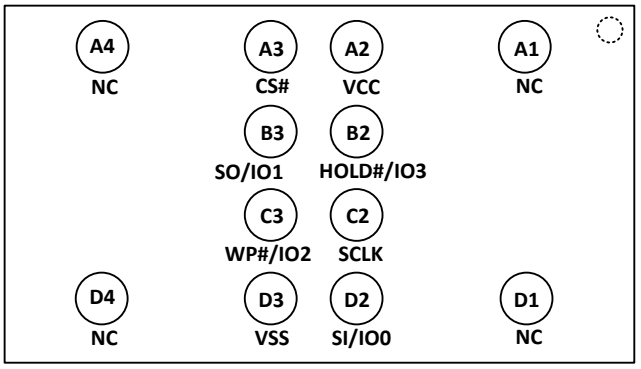


WSON8

TOP VIEW

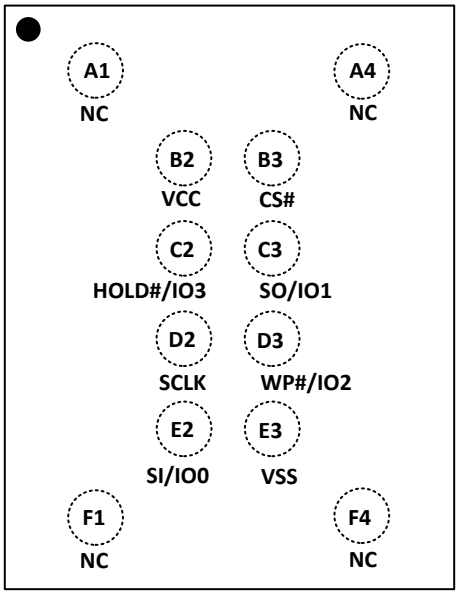


BOTTOM VIEW

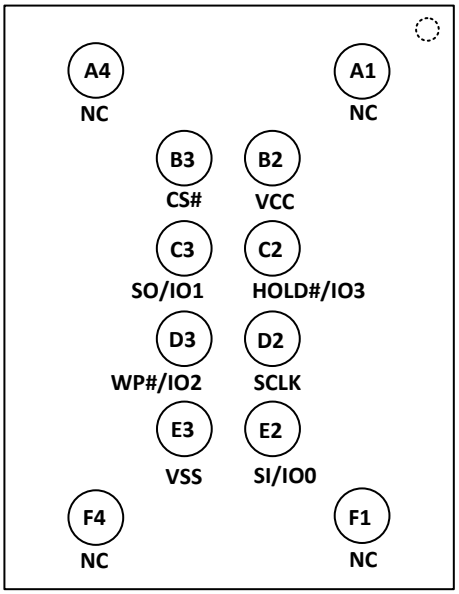


WLCSP-WL

TOP VIEW



BOTTOM VIEW



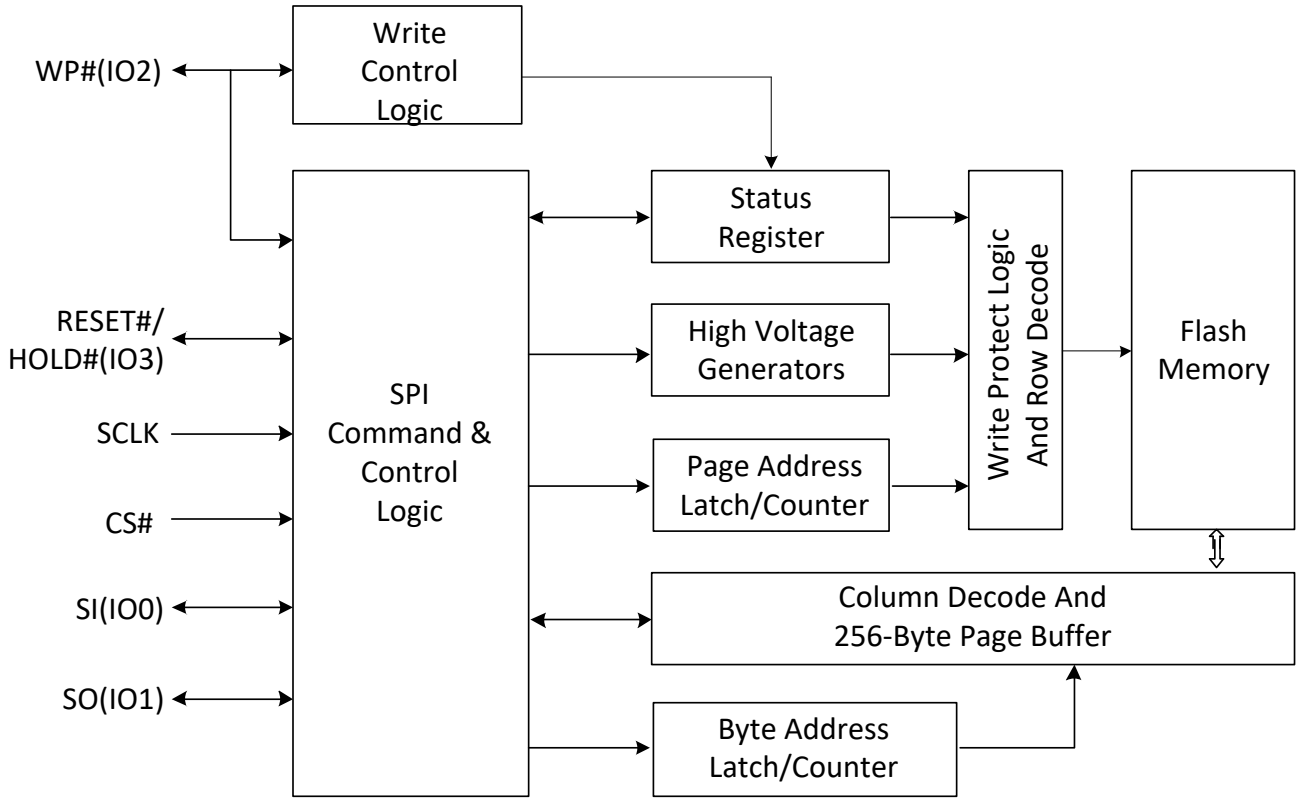
WLCSP-LC

1.3. Pin Description

Pin Name	I/O	Description
CS#	I	Chip Select Input
SO (IO1)	I/O	Data Output (Data Input Output 1)
WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
VSS		Ground
SI (IO0)	I/O	Data Input (Data Input Output 0)
SCLK	I	Serial Clock Input
HOLD#/RESET# (IO3)	I/O	Hold or Reset Input (Data Input Output 3)
VCC		Power Supply

Notes:
1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, WP# & HOLD# (or Reset#) functions are only available for Standard/Dual SPI.

1.4. Block Diagram



1.5. Memory Description

Uniform Block Sector Architecture

Block(64K-byte)	Block(32K-byte)	Sector(4K-byte)	Address Range	
127	255	2047	7FF000H	7FFFFFH
		……	……	……
		2040	7F8000H	7F8FFFH
	254	2039	7F7000H	7F7FFFH
		……	……	……
		2032	7F0000H	7F0FFFH
126	253	2031	7EF000H	7EFFFFH
		……	……	……
		2024	7E8000H	7E8FFFH
	252	2023	7E7000H	7E7FFFH
		……	……	……
		2016	7E0000H	7E0FFFH
	……	……	……	……
		……	……	……
		……	……	……
1	3	31	01F000H	01FFFFH
		……	……	……
		24	018000H	018FFFH
	2	23	017000H	017FFFH
		……	……	……
		16	010000H	010FFFH
0	1	15	00F000H	00FFFFH
		……	……	……
		8	008000H	008FFFH
	0	7	007000H	007FFFH
		……	……	……
		0	000000H	000FFFH

2. DEVICE OPERATION

2.1. SPI Mode

Standard SPI

The device features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The device supports Dual SPI operation when using the "Dual Output Fast Read" and "Dual I/O Fast Read" (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The device supports Quad SPI operation when using the "Quad Output Fast Read"," Quad I/O Fast Read","DTR Fast Read Quad I/O" (6BH, EBH, EDH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

2.2. QPI Mode

The device supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the "Enable the QPI (38H)" command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. "Enable the QPI (38H)" and "Disable the QPI (FFH)" commands are used to switch between these two modes. Upon power-up and after software reset using "Enable Chip Reset (66H)" and "Reset (99H)" command, the default state of the device is Standard/Dual/Quad SPI mode. The QPI mode requires the non-volatile Quad Enable bit (QE) in Status Register to be set.

2.3. DTR Read

To effectively improve the read operation throughput without increasing the serial clock frequency, the device introduces multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

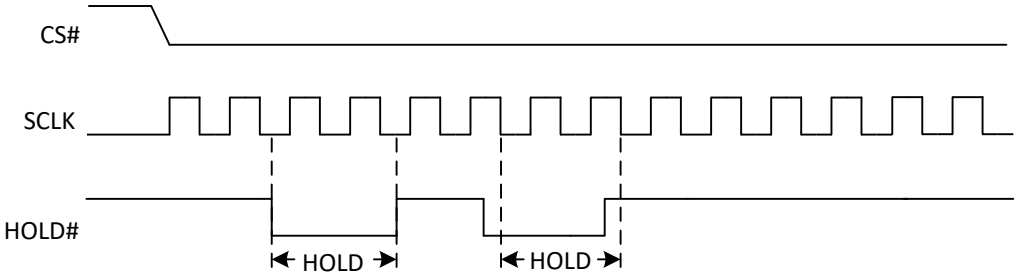
2.4. Hold Function

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Hold Condition



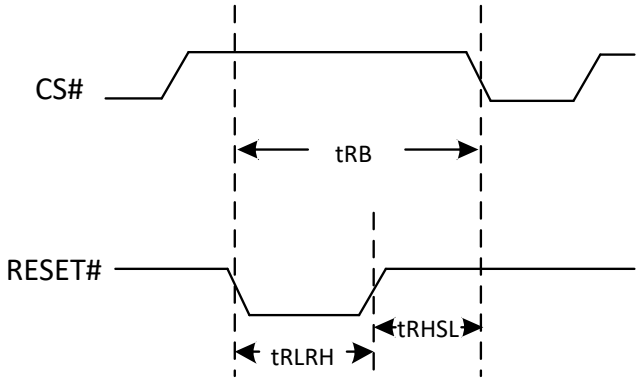
2.5. RESET Function

The RESET# pin allows the device to be reset by the control. The pin 7 can be configured as a RESET# pin depending on the status register setting, which need QE=0 and HOLD/RST=1.

The RESET# pin goes low for a period of tRLRH or longer will reset the flash. After reset cycle, the flash is at the following states:

- Standby mode.
- All the volatile bits will return to the default status as power on.

Reset Timing



Symbol	Parameter	Min	Typ	Max	Unit.
tRLRH	Reset Pulse Width	1			us
tRHSL	Reset High Time Before Read	200			us
tRB	Reset Recovery Time			1	ms

2.6. The Reset Signaling Protocol (JEDEC 252)

The protocol consists of two phases: reset request, and completion (a device internal reset).

Reset Request

1. CS# is driven active low to select the SPI slave (Note1)
2. Clock (SCK) remains stable in either a high or low state (Note 2)
3. SI / IO0 is driven low by the bus master, simultaneously with CS# going active low, (Note 3)
4. CS# is driven inactive (Note 4).

Repeat the steps 1-4 each time alternating the state of SI (Note 5).

NOTE 1 This powers up the SPI slave.

NOTE 2 This prevents any confusion with a command, as no command bits are transferred (clocked).

NOTE 3 No SPI bus slave drives SI during CS# low before a transition of SCK, i.e., slave streaming output active is not allowed until after the first edge of SCK.

NOTE 4 The slave captures the state of SI on the rising edge of CS#.

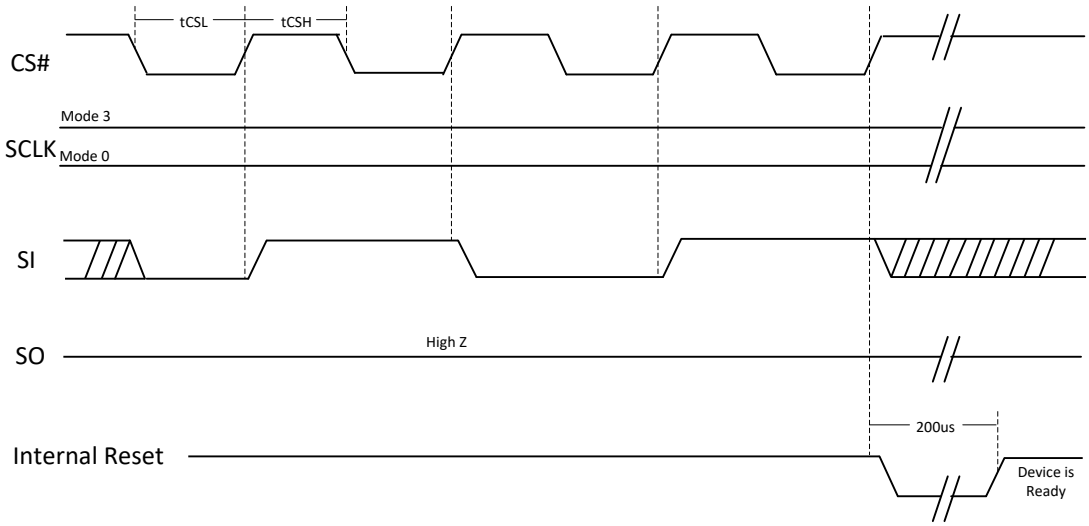
NOTE 5 SI is low on the first CS#, high on the second, low on the third, high on the fourth (This provides a 5h pattern, to differentiate it from random noise).

Reset Completion

After the fourth CS# pulse, the slave triggers its internal reset.

Timing Diagram and Timing Parameters

Reset Signaling Protocol



3. STATUS REGISTER

Status Register-1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP
Status Register Protection Bit	Block Protect Bit	Block Protect Bit	Block Protect Bit	Block Protect Bit	Block Protect Bit	Write Enable Latch	Erase/Write In Progress
Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Volatile, Read Only	Volatile, Read Only

Status Register-2

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	CMP	LB3	LB2	LB1	SUS2	QE	SRP1
Erase Suspend	Complement Protect Bit	Security Register Lock Bit	Security Register Lock Bit	Security Register Lock Bit	Program Suspend	Quad Enable	Status Register Protection Bit
Volatile, Read Only	Non-volatile	Non-volatile writable (OTP)	Non-volatile writable (OTP)	Non-volatile writable (OTP)	Volatile, Read Only	Non-volatile	Non-volatile

Status Register-3

S23	S22	S21	S20	S19	S18	S17	S16
Hold/RST	DRV1	DRV0	Reserved	Reserved	WPS	LC1	Reserved
HOLD# or Reset# Function	Output Driver Strength	Output Driver Strength	Reserved	Reserved	Write protection selection	Latency Code	Reserved
Non-volatile	Non-volatile	Non-volatile	Reserved	Reserved	Non-volatile	Non-volatile writable	Reserved

HOLD/RST

The HOLD/RST bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0, the pin acts as HOLD#, When the HOLD/RST=1, the pin acts as RESET#. However, the HOLD# or RESET# function are only available when QE=0, If QE=1, The HOLD# and RESET# functions are disabled, the pin acts as dedicated data I/O pin.

DRV1, DRV0

The Output Driver Strength (DRV1 & DRV0) bits are used to determine the output driver strength for the Read operations.

DRV1	DRV0	Driver Strength
0	0	25%
0	1	50%
1	0	75% (default)
1	1	100%

WPS

The WPS Bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, BP (4:0) bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

LC

The Latency Code (LC) selects the mode and number of dummy cycles between the end of address and the start of read data output for command EDH under SPI/QPI modes and command 0EH under QPI mode.

Some read commands send mode bits following the address to indicate that the next command will be of the same type with an implied, rather than an explicit instruction. The next command thus does not provide an instruction Byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands.

Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional latency cycles as the SCLK frequency is increased.

Latency Code and DTR Mode Frequency Table

LC	Quad IO DTR Read EDH	DTR Burst Read With Wrap 0EH	Read Clock Frequency (MHz)
0	8 (Default)	8 (Default)	96
1	6	6	72

SUS1, SUS2

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing an Program/Erase Suspend (75H) command (The Erase Suspend will set the SUS1 to 1,and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Program/Erase Resume (7AH) command, software reset (66H+99H) command as well as a power-down, power-up cycle.

CMP

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status register Memory Protection table for details. The default setting is CMP=0.

LB1, LB2, LB3

The LB1, LB12, LB3 bits are non-volatile One Time Program (OTP) bits in Status Register (S11-S13) that provide the write protect control and status to the Security Registers. The default state of LB1-LB3 are 0, the security registers are unlocked. The LB1-LB3 bits can be set to 1 individually using the Write Register instruction. The LB1-LB3 bits are One Time Programmable, once its set to 1, the Security Registers will become read-only permanently.

QE

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground).

SRP1, SRP0

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the type of write protection: software protection, hardware protection, power supply lock-down or one-time programmable protection.

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1. (Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle. Note 1
1	1	X	One-Time Program Note 2	Status Register is protected and cannot be written to.

NOTE:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact XTX for details.

BP4, BP3, BP2, BP1, BP0

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1)becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect(BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, BP0) bits are 1 and CMP=1.

WEL

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

WIP

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

4. DATA PROTECTION

The device provide the following data protection methods:

- Write Enable (WREN) command: The WREN command sets the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up / Software Reset (66H+99H)
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
  - Erase Security Register / Program Security Register
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits, WPS bit and CMP bit define the section of the memory array that can be read but cannot be changed.
- Hardware Protection Mode: WP# goes low to prevent writing status register.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command (ABH) and software reset (66H+99H).

Table1.0 XT25Q64D Protected area size (WPS=0, CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 to 127	7E0000H-7FFFFFH	128KB	Upper 1/64
0	0	0	1	0	124 to 127	7C0000H-7FFFFFH	256KB	Upper 1/32
0	0	0	1	1	120 to 127	780000H-7FFFFFH	512KB	Upper 1/16
0	0	1	0	0	112 to 127	700000H-7FFFFFH	1MB	Upper 1/8
0	0	1	0	1	96 to 127	600000H-7FFFFFH	2MB	Upper 1/4
0	0	1	1	0	64 to 127	400000H-7FFFFFH	4MB	Upper 1/2
0	1	0	0	1	0 to 1	000000H-01FFFFH	128KB	Lower 1/64
0	1	0	1	0	0 to 3	000000H-03FFFFH	256KB	Lower 1/32
0	1	0	1	1	0 to 7	000000H-07FFFFH	512KB	Lower 1/16
0	1	1	0	0	0 to 15	000000H-0FFFFFH	1MB	Lower 1/8
0	1	1	0	1	0 to 31	000000H-1FFFFFH	2MB	Lower 1/4
0	1	1	1	0	0 to 63	000000H-3FFFFFH	4MB	Lower 1/2
X	X	1	1	1	0 to 127	000000H-7FFFFFH	8MB	ALL
1	0	0	0	1	127	7FF000H-7FFFFFH	4KB	Top Block
1	0	0	1	0	127	7FE000H-7FFFFFH	8KB	Top Block
1	0	0	1	1	127	7FC000H-7FFFFFH	16KB	Top Block
1	0	1	0	X	127	7F8000H-7FFFFFH	32KB	Top Block
1	0	1	1	0	127	7F8000H-7FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block

1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

Table1.1 XT25Q64D Protected area size (WPS=0, CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	ALL	000000H-7FFFFFH	ALL	ALL
0	0	0	0	1	0 to 125	000000H-7DFFFFH	8064KB	Lower 63/64
0	0	0	1	0	0 to 123	000000H-7BFFFFH	7936KB	Lower 31/32
0	0	0	1	1	0 to 119	000000H-77FFFFH	7680KB	Lower 15/16
0	0	1	0	0	0 to 111	000000H-6FFFFFH	7MB	Lower 7/8
0	0	1	0	1	0 to 95	000000H-5FFFFFH	6MB	Lower 3/4
0	0	1	1	0	0 to 63	000000H-3FFFFFH	4MB	Lower 1/2
0	1	0	0	1	2 to 127	020000H-7FFFFFH	8064KB	Upper 63/64
0	1	0	1	0	4 to 127	040000H-7FFFFFH	7936KB	Upper 31/32
0	1	0	1	1	8 to 127	080000H-7FFFFFH	7680KB	Upper 15/16
0	1	1	0	0	16 to 127	100000H-7FFFFFH	7MB	Upper 7/8
0	1	1	0	1	32 to 127	200000H-7FFFFFH	6MB	Upper 3/4
0	1	1	1	0	64 to 127	400000H-7FFFFFH	4MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 127	000000H-7FEFFFH	8188KB	L-2047/2048
1	0	0	1	0	0 to 127	000000H-7FDFFFH	8184KB	L-1023/1024
1	0	0	1	1	0 to 127	000000H-7FBFFFH	8176KB	L-511/512
1	0	1	0	X	0 to 127	000000H-7F7FFFH	8160KB	L-255/256
1	0	1	1	0	0 to 127	000000H-7F7FFFH	8160KB	L-255/256
1	1	0	0	1	0 to 127	001000H-7FFFFFH	8188KB	U-2047/2048
1	1	0	1	0	0 to 127	002000H-7FFFFFH	8184KB	U-1023/1024
1	1	0	1	1	0 to 127	004000H-7FFFFFH	8176KB	U-511/512
1	1	1	0	X	0 to 127	008000H-7FFFFFH	8160KB	U-255/256
1	1	1	1	0	0 to 127	008000H-7FFFFFH	8160KB	U-255/256

Table1.2 XT25Q64D Individual Block Protection (WPS=1)

Block	Sector	Address range		Individual Block Lock Operation
127	2047	7FF000H	7FFFFFH	**The Top/Bottom block is protected by sector.** **Other 126 Blocks are protected by block** **Block Lock:** 36H+Address **Block Unlock:** 39H+Address **Read Block Lock:** 3DH+Address **Global Block Lock:** 7EH **Global Block Unlock:** 98H
	.....	.....	.....	
	2032	7F0000H	7F0FFFH	
.....				
.....				
2				
1				
0	15	00F000H	00FFFFH	
	.....	.....	.....	
	0	000000H	000FFFH	

5. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table 2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable or Write Disable command, CS# must be driven high exactly at the byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 2 Commands

Command Name	Command Code	SPI	QPI	Address Byte					Dummy Cycle	Data Byte
				Total ADD Byte	Byte1	Byte2	Byte3	Byte4		
Register Access										
Read Status Register_1	05H	√	√	0					0	1 to ∞
Read Status Register_2	35H	√	√	0					0	1 to ∞
Read Status Register_3	15H	√	√	0					0	1 to ∞
Write Status Register_1	01H	√	√	0					0	1 or 2
Write Status Register_2	31H	√	√	0					0	1
Write Status Register_3	11H	√	√	0					0	1
Manufacturer/Device ID	90H	√	√	3					0	1 to ∞
Read Serial Flash Discoverable Parameters	5AH	√	√	3	ADD1	ADD2	ADD3		8[Note2]	1 to ∞
Read Unique ID	4BH	√	√	0					32[Note2]	1 to ∞
Read Identification	9FH	√	√	0					0	1 to ∞
Array access										
Read Data	03H	√		3	ADD1	ADD2	ADD3		0	1 to ∞
Fast Read	0BH	√	√	3	ADD1	ADD2	ADD3		8[Note2]	1 to ∞
Dual Output Fast Read	3BH	√		3	ADD1	ADD2	ADD3		8	1 to ∞
Dual I/O Fast Read	BBH	√		3	ADD1	ADD2	ADD3		4	1 to ∞
Quad Output Fast Read	6BH	√		3	ADD1	ADD2	ADD3		8	1 to ∞

Quad I/O Fast Read	EBH	√	√	3	ADD1	ADD2	ADD3		6[Note2 Note3]	1 to ∞
Burst Read with Wrap	0CH		√	3	ADD1	ADD2	ADD3		4/6/8[Note2]	1 to ∞
Quad Read under DTR	EDH	√	√	3	ADD1	ADD2	ADD3		8/6 [Note4]	1 to ∞
DTR Read with Wrap	0EH		√	3	ADD1	ADD2	ADD3		8/6[Note4]	1 to ∞
Page Program	02H	√	√	3	ADD1	ADD2	ADD3		0	1 to 256
Quad Page Program	32H	√		3	ADD1	ADD2	ADD3		0	1 to 256
Extended Quad Input Fast Program	C2h	√		3	ADD1	ADD2	ADD3		0	1 to 256
4KB Sector Erase	20H	√	√	3	ADD1	ADD2	ADD3		0	0
32KB Block Erase	52H	√	√	3	ADD1	ADD2	ADD3		0	0
64KB Block Erase	D8H	√	√	3	ADD1	ADD2	ADD3		0	0
Chip Erase	C7/60H	√	√	0					0	0
Device Operations										
Enable Reset	66H	√	√	0					0	0
Reset	99H	√	√	0					0	0
Write Enable	06H	√	√	0					0	0
Write Enable for Volatile Status Register	50H	√	√	0					0	0
Write Disable	04H	√	√	0					0	0
Program Erase Suspend	75H	√	√	0					0	0
Program Erase Resume	7AH	√	√	0					0	0
Enable QPI	38H	√		0					0	0
Disable QPI	FFH		√	0					0	0
Set Burst with Wrap	77H	√		0					0	0
Set Read Parameters	C0H		√	0					0	0
Continuous Read Reset	FFH[Note1]	√	√							
Deep Power-Down	B9H	√	√	0					0	0
Release From Deep Power-Down	ABH	√	√	0					0	0
Release From Deep Power-Down/Read Device ID	ABH	√	√	0					24[Note2]	1 to ∞
One-Time Programmable (OTP) Operations										

Erase Security Register	44H	√	√	3	ADD1	ADD2	ADD3		0	0
Program Security Register	42H	√	√	3	ADD1	ADD2	ADD3		0	1 to 256
Read Security Register	48H	√	√	3	ADD1	ADD2	ADD3		8 Note2	1 to ∞
Advanced Sector Protection Operations										
Global Block Lock	7EH	√	√	0					0	0
Global Block Unlock	98H	√	√	0					0	0
Individual Block Lock	36H	√	√	3	ADD1	ADD2	ADD3		0	0
Individual Block Unlock	39H	√	√	3	ADD1	ADD2	ADD3		0	0
Read Block Lock	3DH	√	√	3	ADD1	ADD2	ADD3		0	1

Note1:
Under SPI mode and Continuous Read Mode , Command FFH will exit the Continuous Read mode.

Under QPI mode and Continuous Read Mode , The first time sending command FFH will exit the Continuous Read mode, the second time sending FFH will exit QPI mode.

Note2:

In QPI mode, the number of dummy clocks is con-figured by the “Set Read Parameters (C0H)” command. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Note3:

M7-0 is counted for dummy clocks.

Note4:

For EDH at both SPI mode and QPI mode, and for 0EH under QPI mode, the number of dummy clocks is con-figured by the LC bit. The number of dummy clocks can be configured as either 8/6.

Table of ID Definitions:

XT25Q64D

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	0B	60	17
90H	0B		16
ABH			16

5.1. Register Access

5.1.1. Read Status Register (05H or 35H or 15H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. For the command code “35H”, the SO will output Status Register bits S15~S8. For the command code “15H”, the SO will output Status Register bits S23~S16.

Figure 1. Read Status Register Sequence Diagram

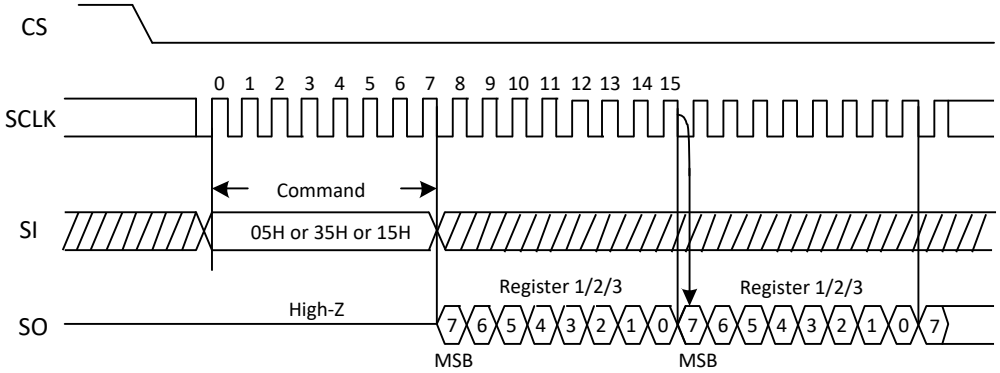
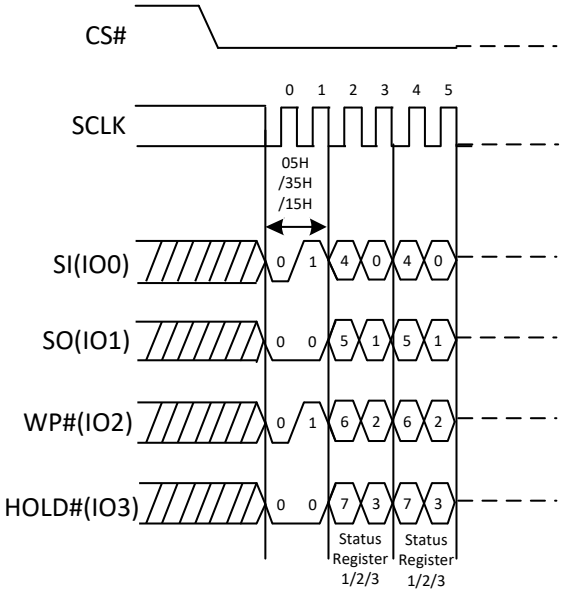


Figure 1a. Read Status Register Sequence Diagram (QPI)



5.1.2. Write Status Register (01H or 31H or 11H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on the volatile bits of the Status Register. CS# must be driven high after the eighth bit or the sixteenth of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 1.0 & 1.1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered. For command code “01H”, the SI will input Status Register bits S7~S0 and S15~S8. For the command code “31H”, the SI will input Status Register bits S15~S8. For the command code “11H”, the SI will input Status Register bits S23~S16.

Figure 2. Write Status Register Sequence Diagram

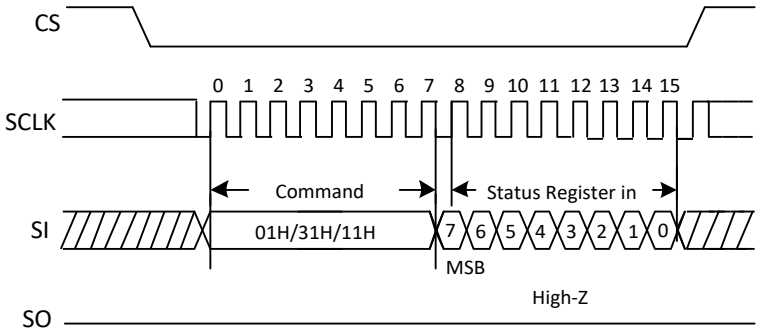


Figure 2a. Write Status Register Sequence Diagram (QPI)

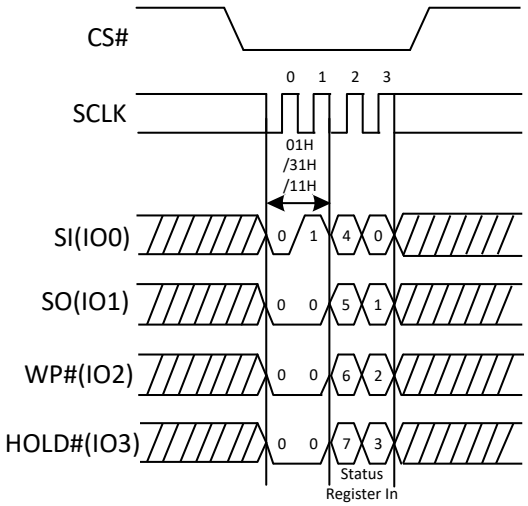


Figure2b.Write Status Register Sequence Diagram

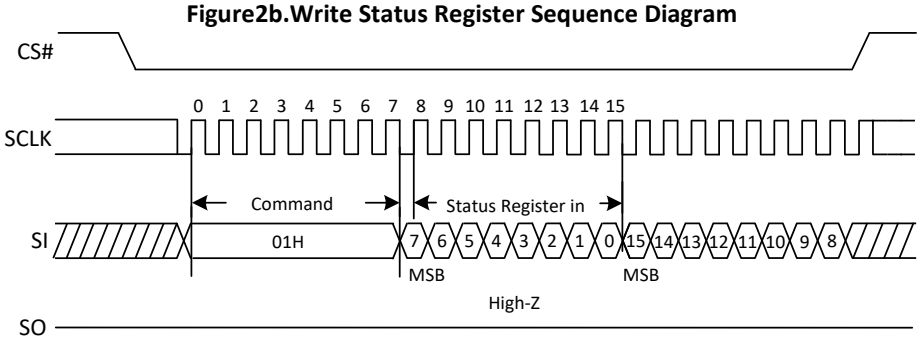
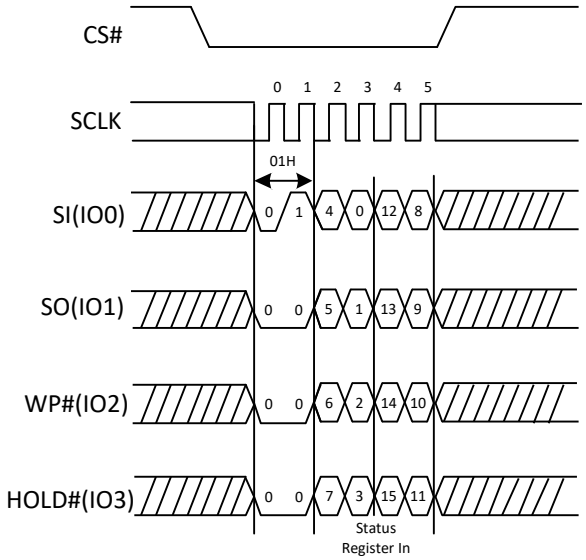


Figure2c. Write Status Register Sequence Diagram (QPI)



5.1.3. Read Manufacture ID/ Device ID (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Deep Power-Down and Read Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in Figure 3. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 3. Read Manufacture ID/ Device ID Sequence Diagram

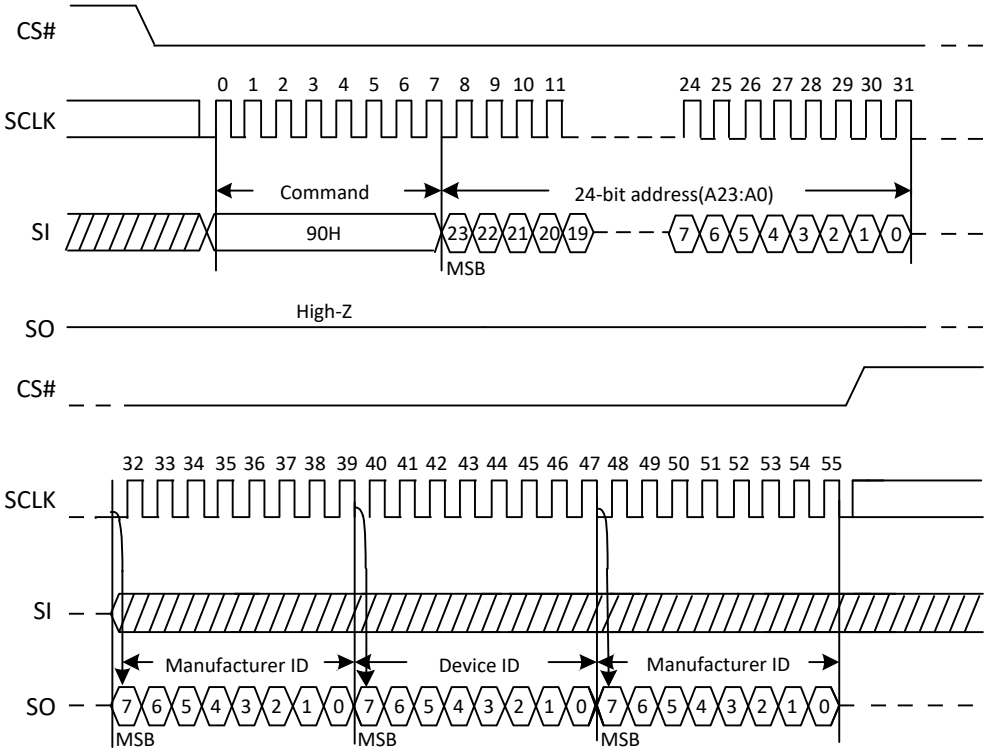
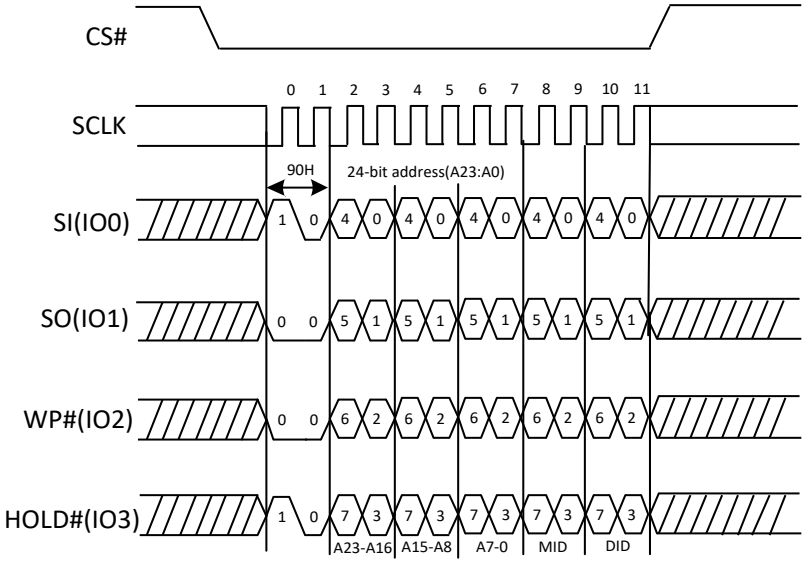


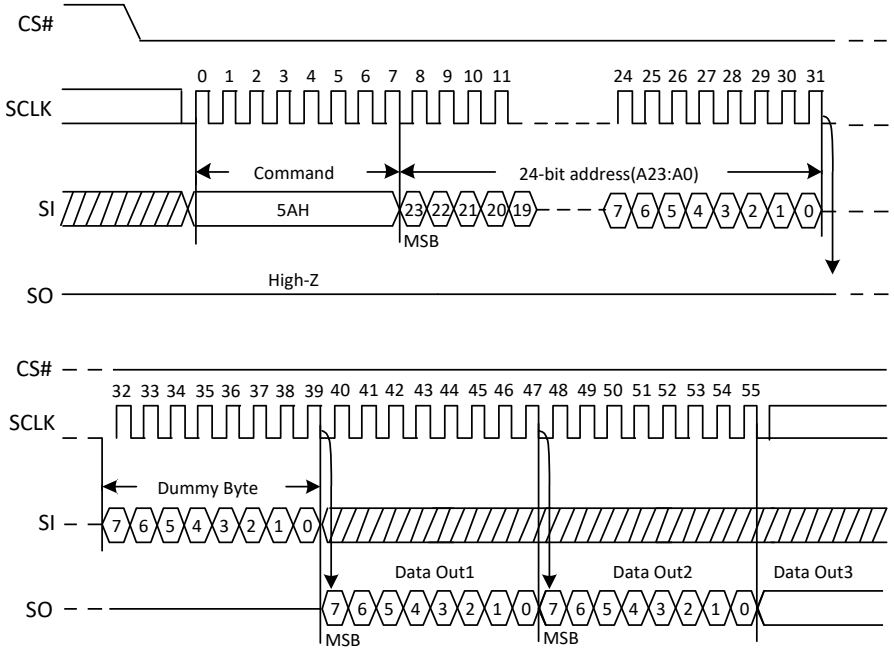
Figure 3a. Read Manufacture ID/ Device ID Sequence Diagram (QPI)



5.1.4. Read SFDP(5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

Figure 4. Read Serial Flash Discoverable Parameter command Sequence Diagram

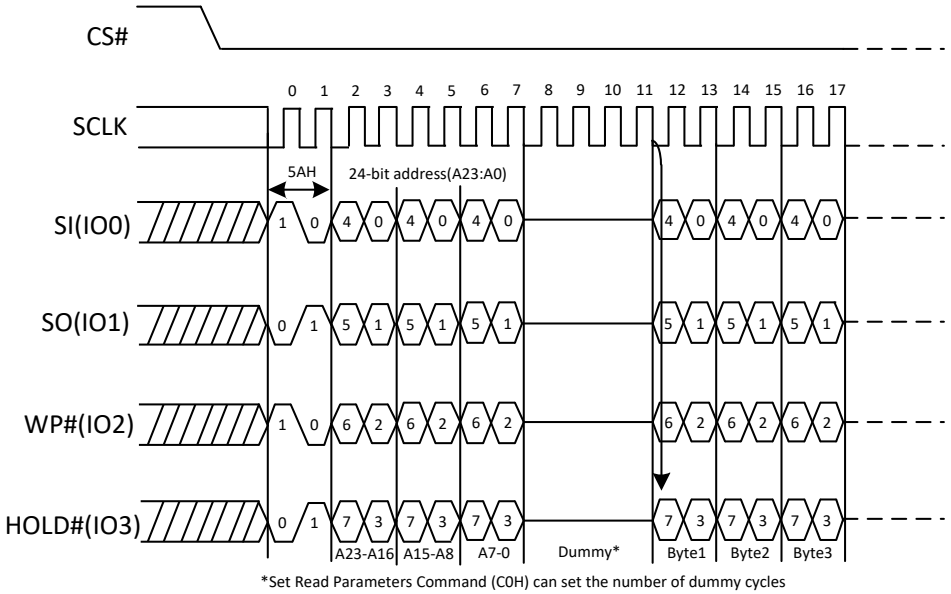


Note: A23-A8 = 0, A7-A0 is the starting byte address for 256-byte SFDP Register.

Read Serial Flash Discoverable Parameter (5AH) in QPI mode

The Read Serial Flash Discoverable Parameter command is also supported in QPI mode. See the following figure . In QPI mode, the number of dummy clocks is configured by the “Set Read Parameters (C0H)” command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Figure 4a. Read Serial Flash Discoverable Parameter command Sequence Diagram (QPI)



*Set Read Parameters Command (C0H) can set the number of dummy cycles

Table 4. Parameter Table (0): Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H Follow JESD216B standard	04H	07:00	06H	06H
SFDP Major Revision Number	Start from 01H Follow JESD216B standard	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 00H Follow JESD216B standard	09H	15:08	06H	06H
Parameter Table Major Revision Number	Start from 01H Follow JESD216B standard	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	10H	10H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number (XTX Manufacturer ID)	It is indicates XTX manufacturer ID	10H	07:00	0BH	0BH
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of XTX Flash Parameter table	14H	07:00	90H	90H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Parameter Table (1): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: Not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: Buffer size = 1Byte or <64Byte(32 Words) 1: Buffer Size = 64Byte(32 Words) or larger		02	1b	
Volatile Status Register Block Protect bits	0: Nonvolatile status bit, support 06H and 50H 1: Volatile status bit		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1-2) Fast Read	0 = NOT supported 1 = supported	32H	16	1b	F9H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0 = NOT supported 1 = supported		19	1b	
(1-2-2) Fast Read	0 = NOT supported 1 = supported		20	1b	
(1-4-4) Fast Read	0 = NOT supported 1 = supported		21	1b	
(1-1-4) Fast Read	0 = NOT supported 1 = supported		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	03FFFFFFH	
(1-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support 0 0100b: 4 Dummy Clocks (M7-M0 excluded)	38H	04:00	00100b	44H
(1-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support 010b: 8bit Mode Bits = 2 Dummy Clocks (M7-M0)		07:05	010b	
(1-4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support 0 1000b: 8 Dummy Clocks	3AH	20:16	01000b	08H
(1-1-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	6BH	6BH

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support 0 1000b: 8 Dummy Clocks	3CH	04:00	01000b	08H
(1-1-2) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcodex		3DH	15:08	3BH	3BH
(1-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support (M7-M0 excluded)	3EH	20:16	00000b	80H
(1-2-2) Fast Read Number of Mode Bits	000b:Mode Bits not support 100b: 8bit Mode Bits = 4 Dummy Clocks (M7-M0)		23:21	100b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0 = NOT supported 1 = supported	40H	00	0b	FEH
Unused			03:01	111b	
(4-4-4) Fast Read	0 = NOT supported 1 = supported		04	1b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4-4) Fast Read Number of Wait states(QPI)	0 0000b: Wait states (Dummy Clocks) not support 0 0110b: 6 Dummy Clocks (M7-M0 excluded)	4AH	20:16	00110b	46H
(4-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support 010b: 8bit Mode Bits = 2 Dummy Clocks (M7-M0)		23:21	010b	
(4-4-4) Fast Read Opcode		4BH	31:24	EBH	EBH
Erase Type 1 Size (4Kb)	Sector/block size=2^N Bytes 0x00b: this sector type don't exist	4CH	07:00	0CH	0CH
Erase Type 1 Opcode		4DH	15:08	20H	20H
Erase Type 2 Size (32Kb)	Sector/block size=2^N Bytes 0x00b: this sector type don't exist	4EH	23:16	0FH	0FH
Erase Type 2 Opcode		4FH	31:24	52H	52H
Erase Type 3 Size (64Kb)	Sector/block size=2^N Bytes 0x00b: this sector type don't exist	50H	07:00	10H	10H
Erase Type 3 Opcode		51H	15:08	D8H	D8H
Erase Type 4 Size (256Kb)	Sector/block size=2^N Bytes 0x00b: this sector type don't exist	52H	23:16	00H	00H
Erase Type 4 Opcode		53H	31:24	FFH	FFH

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Multiplier from typical erase time to maximum erase time	Erase Type n=1 Maximum erase time = 2*(Count + 1)* Typical Erase Time	54H:55H	3:0	0100b	FEA5 3A24H
Erase Type 1 Erase, Typical time	Erase time=45ms/48ms		8:4	00010b	
			10:9	01b	
Erase Type 2 Erase, Typical time	Erase time=120ms/128ms		15:11	00111b	
		56H:57H	17:16	01b	
Erase Type 3 Erase, Typical time	Erase time=150ms/160ms		22:18	01001b	
			24:23	01b	
Erase Type 4 Erase, Typical time	Not exist		31:25	1111111b	
Multiplier from typical time to max time for Page or Byte program	Maximum Page program time = 2*(Count + 1)* Typical Time	58H	3:0	0001b	81H
Page Size	Page size=256Byte		7:4	1000b	
Page Program Typical time	Page program=400us/448us	59H	13:8	100110b	E6H
Byte Program Typical time, first Byte	First Byte program=30us/32us		15:14	11b	
		5AH	18:16	100b	14H
Byte Program Typical time, additional Byte	Additional Byte program=2.5us/3us		23:19	00010b	
Chip Erase, Typical time	Chip erase typical time=20s/20s	5BH	30:24	1000100b	44H
Reserved			31	0b	
Prohibited Operations During Program Suspend		5CH	3:0	1000b	A8H
Prohibited Operations During Erase Suspend			7:4	1010b	
Reserved		5DH	8	0b	62H
Program Resume to Suspend Interval	Interval=100us/128us		12:9	0001b	
Suspend in-progress program max latency	max latency=20us/20us		15:13	011b	
		5EH	19:16	0110b	16H
Erase Resume to Suspend Interval	Interval=100us/128us		23:20	0001b	
Suspend in-progress erase max latency	max latency=20us/20us	5FH	30:24	0110011b	33H
Suspend / Resume supported	0=supported 1=NOT supported		31	0b	
Program Resume Instruction		60H	7:0	7AH	7AH
Program Suspend Instruction		61H	15:0	75H	75H
Resume Instruction		62H	23:16	7AH	7AH
Suspend Instruction		63H	31:24	75H	75H

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Reserved		64H	1:0	11b	F7H
Status Register Polling Device Busy	Use of legacy polling is supported by reading the Status Register with 05h instruction and checking WIP bit[0]		7:2	111101b	
Exit Deep Power-Down to next operation delay	Delay=6us/6us	65H	14:8	0100101b	A5H
Exit Deep Power-Down Instruction	ABH		15	1b	
Enter Deep Power-Down Instruction	B9H	66H	22:16	1010101b	D5H
			23	1b	
Deep Power-Down Supported	0 = supported 1 = NOT supported	67H	30:24	1011100b	5CH
			31	0b	
4-4-4 mode disable sequences	Issue FFH or 66/99H, set 1001b; If QPI not supported, set all bit to 0;	68H	3:0	1001b	19H
4-4-4 mode enable sequences	x_xxx1x: Issue instruction 38H; x_xxxx1: Set QE bit, then issue instruction 38H; If QPI not supported, set all bit to 0;		7:4	0001b	
0-4-4 mode supported	0 = NOT supported 1 = supported	69H	8	0b	B6H
			9	1b	
0-4-4 Mode Exit Method	xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation xx_x1xxb/1x_xxxxb: Reserved xx_1xxxb: Input Fh (mode bit reset) on IO0-IO3 for 8 clocks. This will terminate the mode prior to the next read operation.		15:10	101101b	
0-4-4 Mode Entry Method	xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode. x1xxb: Mode Bit[7:0]=AXh. 1xxxb: Reserved.	6AH	19:16	1101b	4DH
Quad Enable Requirements (QER)	100b: QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Writing one byte to the status register does not modify status register 2.		22:20	100b	
RESET Disable	1=Set Extended Configuration Register bit 4 to disable HOLD or RESET; 0=not support;		23	0b	
Reserved		6BH	31:24	11111111b	FFH

Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1	x1x_xxxxb/1xx_xxxxb: Reserved xxx_1xxxb: Non-Volatile/Volatile status register 1 powers-up to last written value in the non-volatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register.	6CH	6:0	1101000b	E8H
Reserved			7	1b	
Soft Reset and Rescue Sequence Support	66H-99H	6DH	13:8	010000b	10H
Exit 4-Byte Addressing	Reserved		15:14	00b	
		6EH	23:16	00000000b	00H
Enter 4-Bye Addressing	Reserved	6FH	31:24	00000000b	00H

Parameter Table (2): XTX Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	1600H=1.600V 1950H=1.950V 2000H=2.000V 2100H=2.100V 3600H=3.600V	91H:90H	15:00	2000H	2000H
Vcc Supply Minimum Voltage	1140H=1.140V 1650H=1.650V 2700H=2.700V	93H:92H	31:16	1650H	1650H
HW Reset# pin	0 = NOT supported 1 = supported	95H:94H	00	1b	F99FH
HW Hold# pin	0 = NOT supported 1 = supported		01	1b	
Deep Power Down Mode	0 = NOT supported 1 = supported		02	1b	
SW Reset	0 = NOT supported 1 = supported		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H) before Reset command.		11:04	1001 1001b (99H)	
Program Suspend/Resume	0 = NOT supported 1 = supported		12	1b	
Erase Suspend/Resume	0 = NOT supported 1 = supported		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0 = NOT supported 1 = supported		15	1b	
Wrap-Around Read mode Opcode		96H	23:16	77H	77H
Wrap-Around Read data length	08H:support 8Byte wrap-around read 16H:8B&16Byte 32H:8B&16B&32Byte 64H:8B&16B&32B&64Byte	97H	31:24	64H	64H
Individual block lock	0 = NOT supported 1 = supported	9BH:98H	00	1b	E8D9H
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	36H	
Individual block lock Volatile Protect bit default protect status	0=protected 1=unprotected		10	0b	
Secured OTP	0 = NOT supported 1 = supported		11	1b	
Read Lock	0 = NOT supported 1 = supported		12	0b	
Permanent Lock	0 = NOT supported 1 = supported		13	1b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

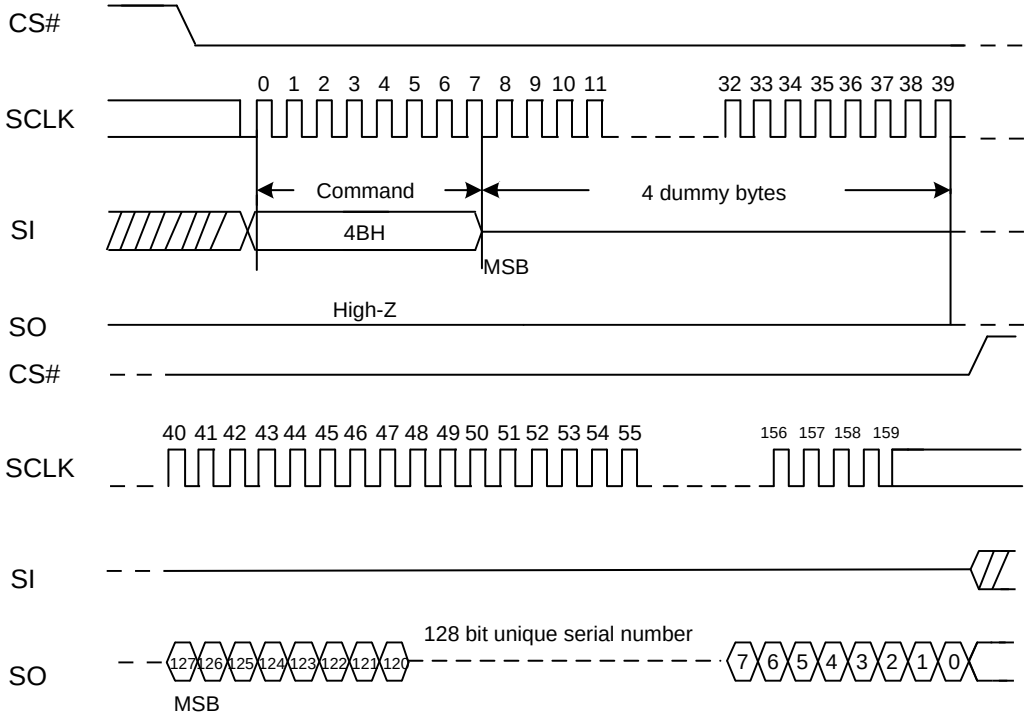
5.1.5. Read Unique ID(4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command →4 dummy bytes → 128bit Unique ID Out → CS# goes high.

The command sequence is show below.

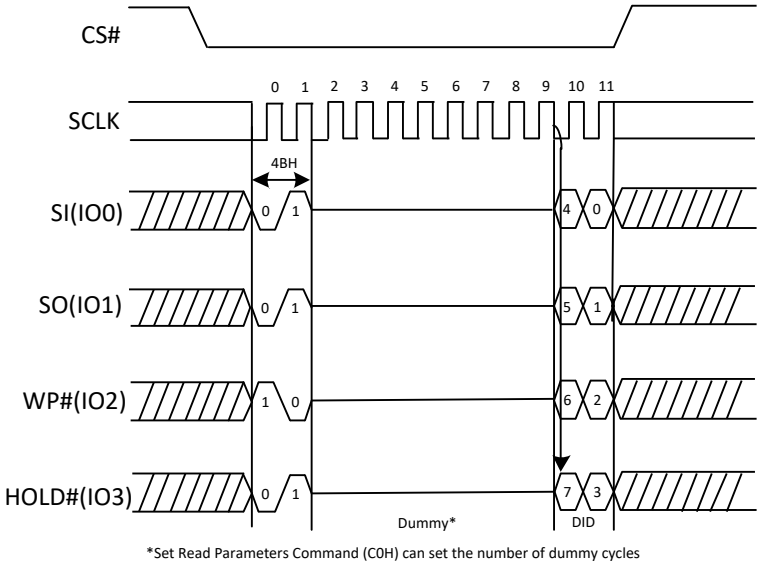
Figure 5. Read Unique ID (RUID) Sequence (Command 4BH)



Read Unique ID (4BH) in QPI mode

The Read Unique ID command is also supported in QPI mode. See the figure below, In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Figure 5a. Read Unique ID (RUID) Sequence (Command 4BH) (QPI)



*Set Read Parameters Command (C0H) can set the number of dummy cycles

5.1.6. Read Identification (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress will not be decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit manufacture identification and device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure 6. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 6. Read Identification ID Sequence Diagram

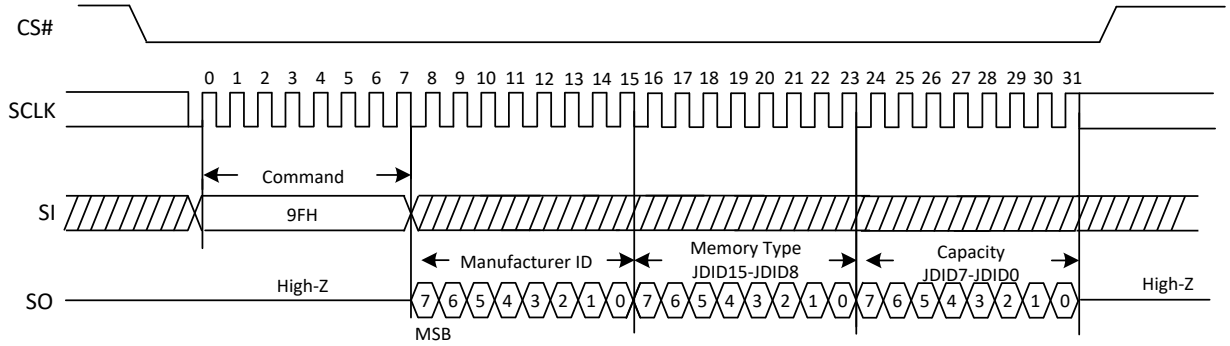
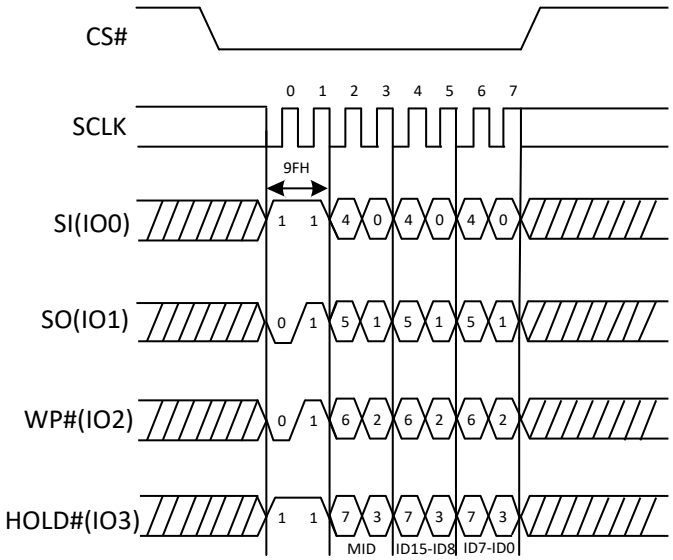


Figure 6a. Read Identification ID Sequence Diagram (QPI)

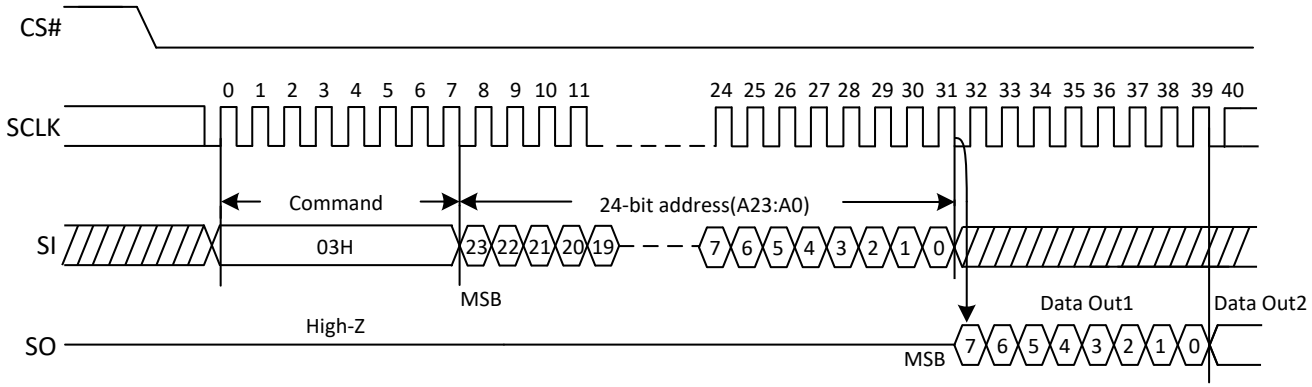


5.2. Array access

5.2.1. Normal Read (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

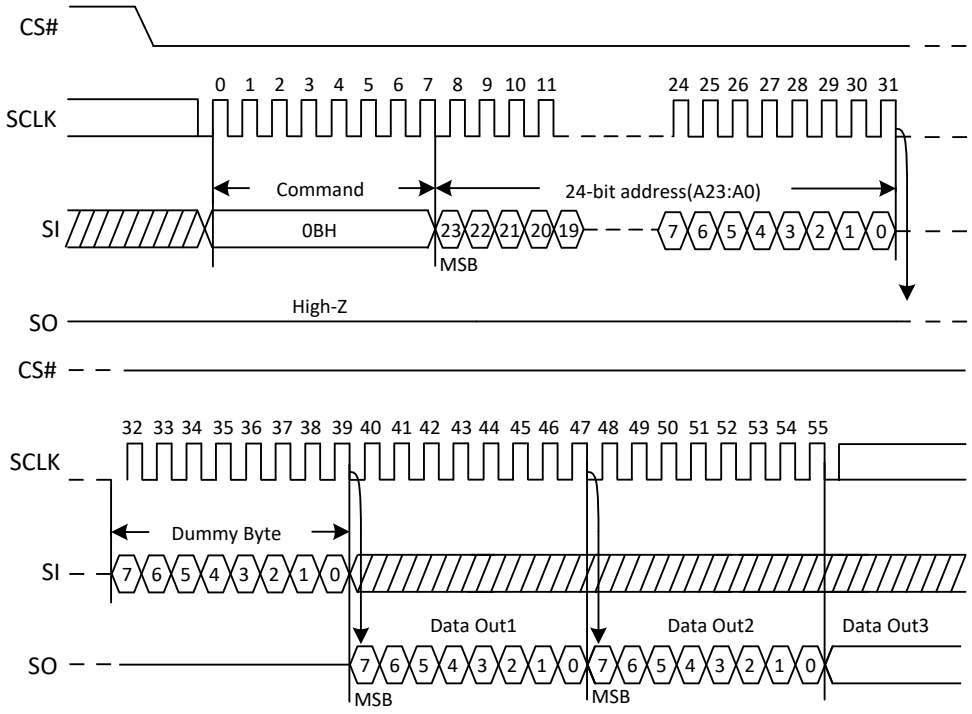
Figure 7.Read Data Bytes Sequence Diagram



5.2.2. Fast Read (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

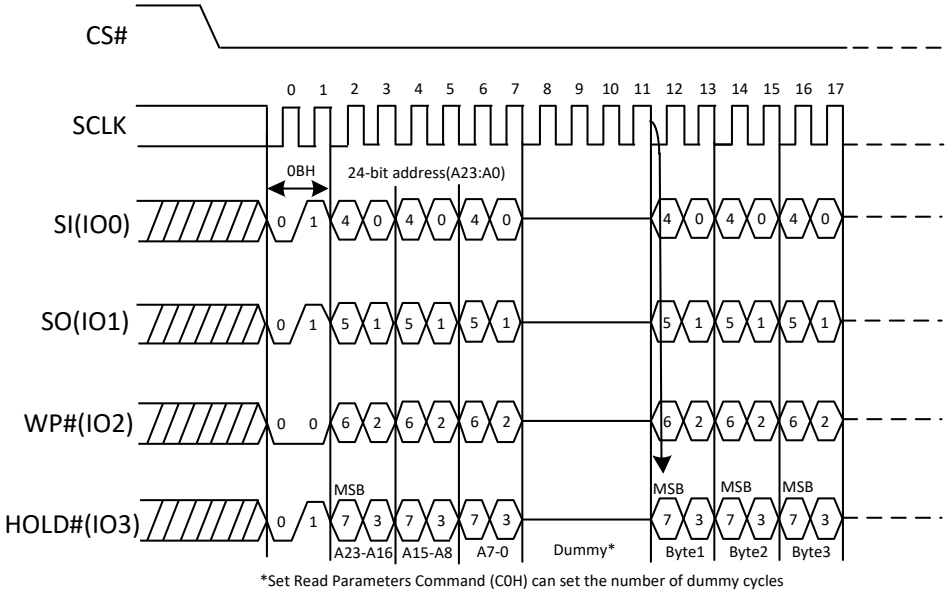
Figure 8. Read Data By test Higher Speed Sequence Diagram



Fast Read (0BH) in QPI mode

The Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Figure 8a. Read Data Bytes at Higher Speed Sequence Diagram (QPI)

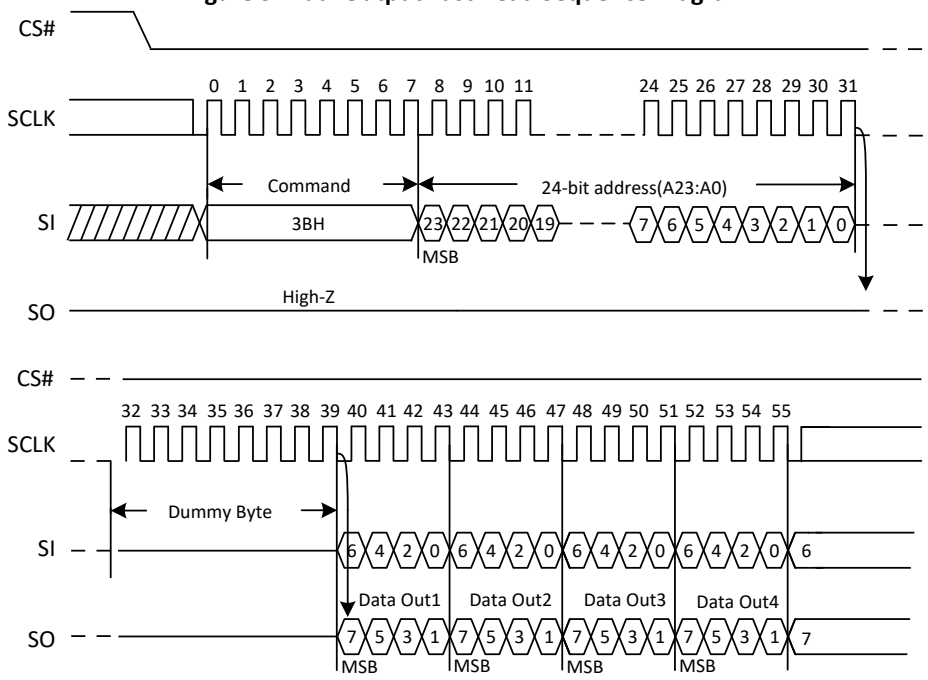


*Set Read Parameters Command (C0H) can set the number of dummy cycles

5.2.3. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in the following figure. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

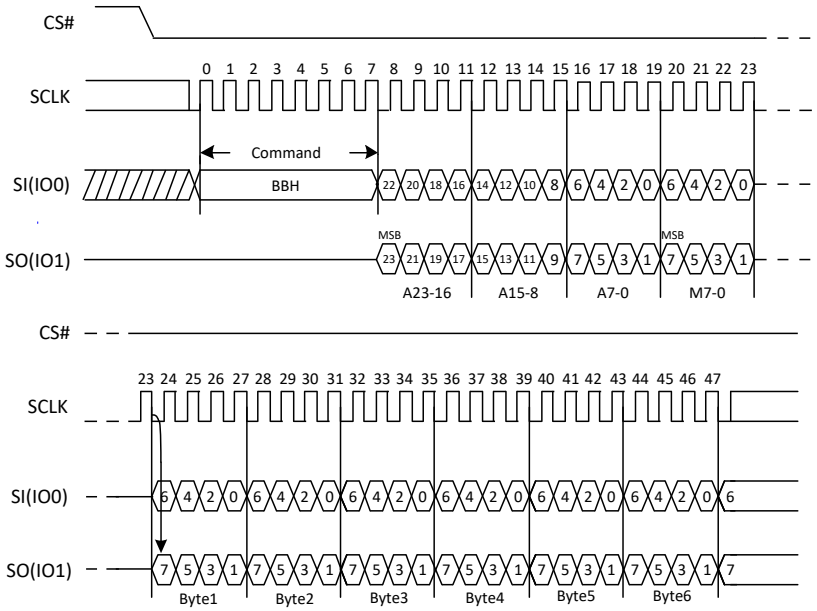
Figure 9. Dual Output Fast Read Sequence Diagram



5.2.4. Dual I/O Fast Read(BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in the following figure. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

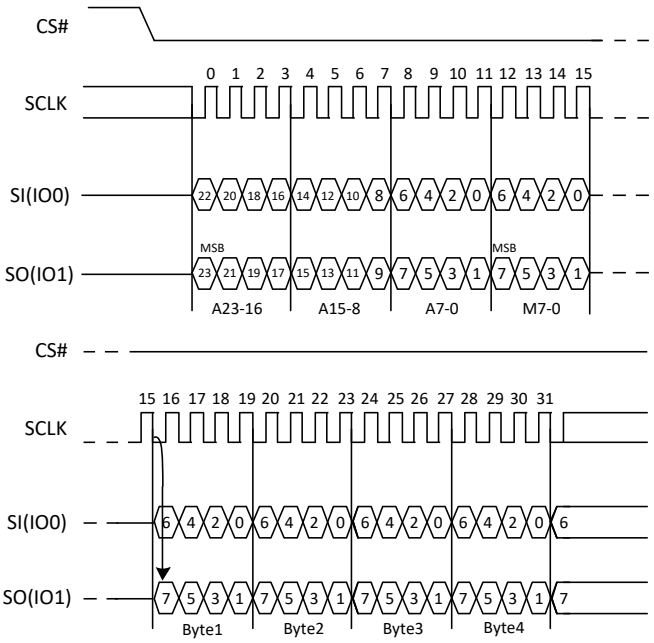
Figure 10. Dual I/O Fast Read Sequence Diagram (M5-4≠(1,0))



Dual I/O Fast Read with "Continuous Read Mode"

The Dual I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) =(1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in figure below. If the "Continuous Read Mode" bits (M5- 4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5- 4) before issuing normal command.

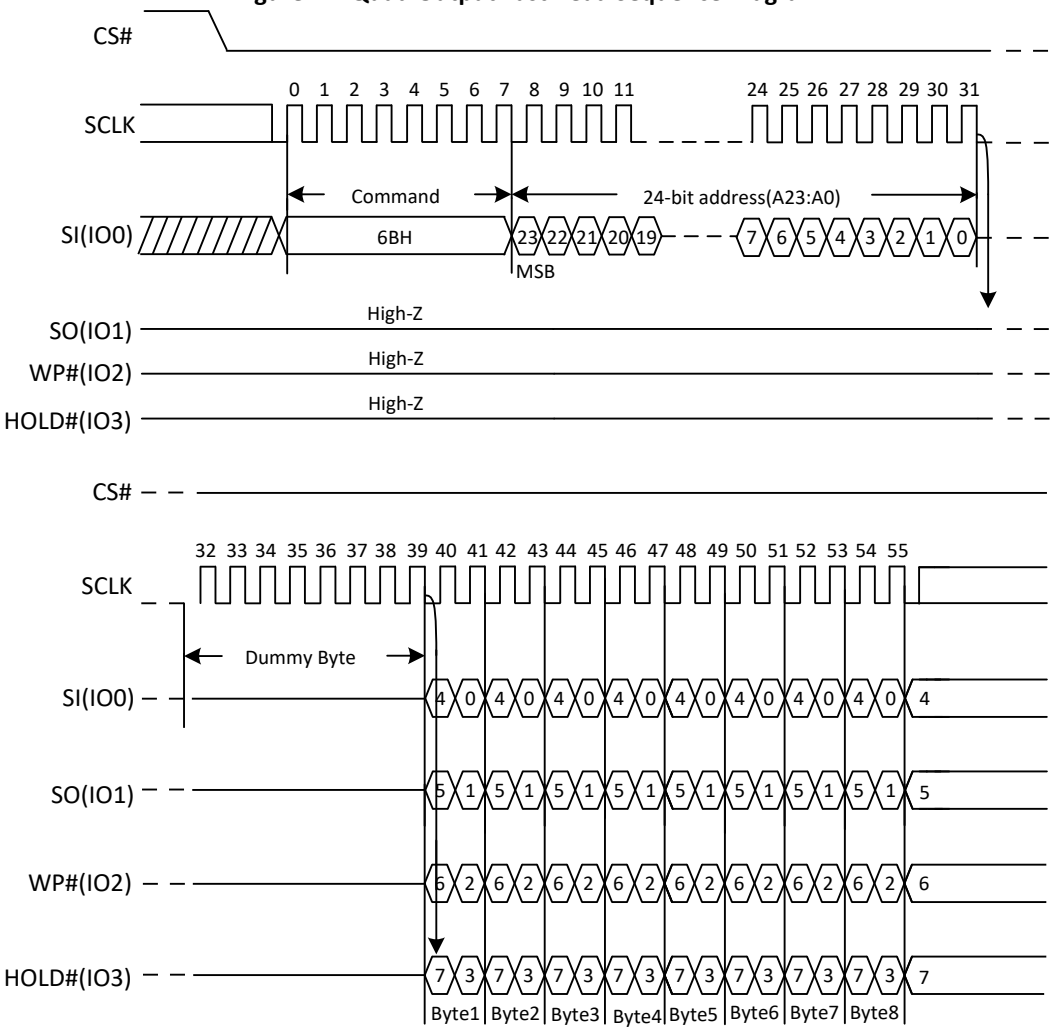
Figure 10a. Dual I/O Fast Read Sequence Diagram (M5-4=(1,0))



5.2.5. Quad Output Fast Read(6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in the figure below. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

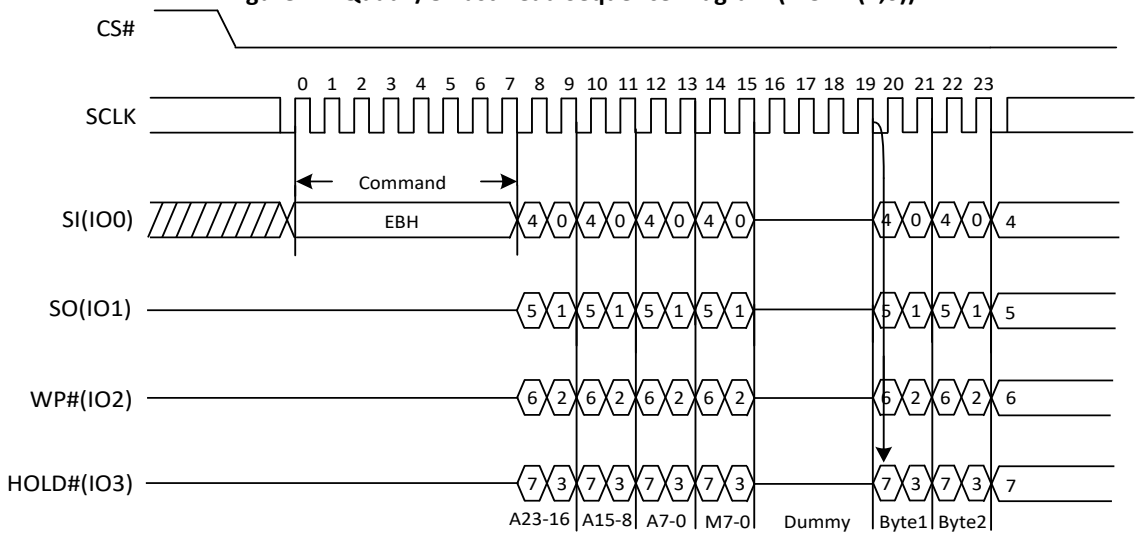
Figure 11. Quad Output Fast Read Sequence Diagram



5.2.6. Quad I/O Fast Read(EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in the figure below. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

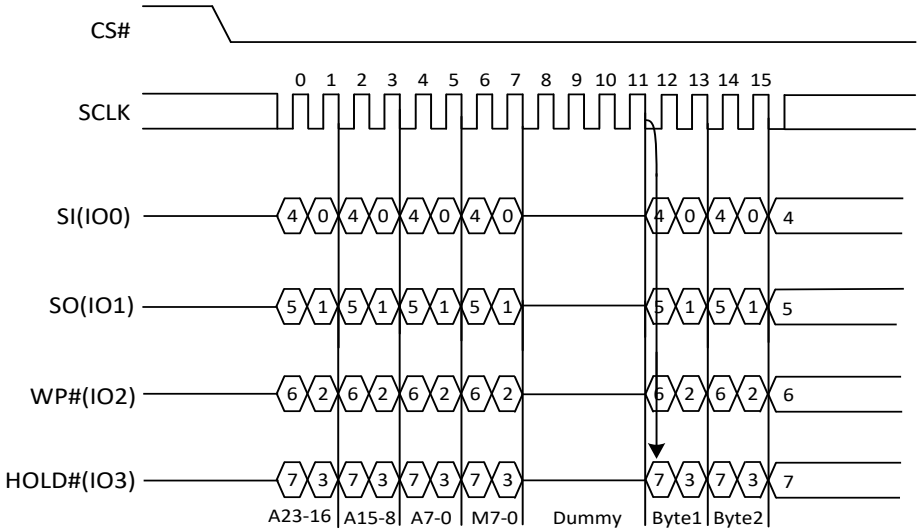
Figure 12. Quad I/O Fast Read Sequence Diagram (M5-4≠(1,0))



Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) =(1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in Figure 12a. If the “Continuous Read Mode” (M5- 4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5- 4) before issuing normal command.

Figure 12a. Quad I/O Fast Read Sequence Diagram (M5-4=(1,0))



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

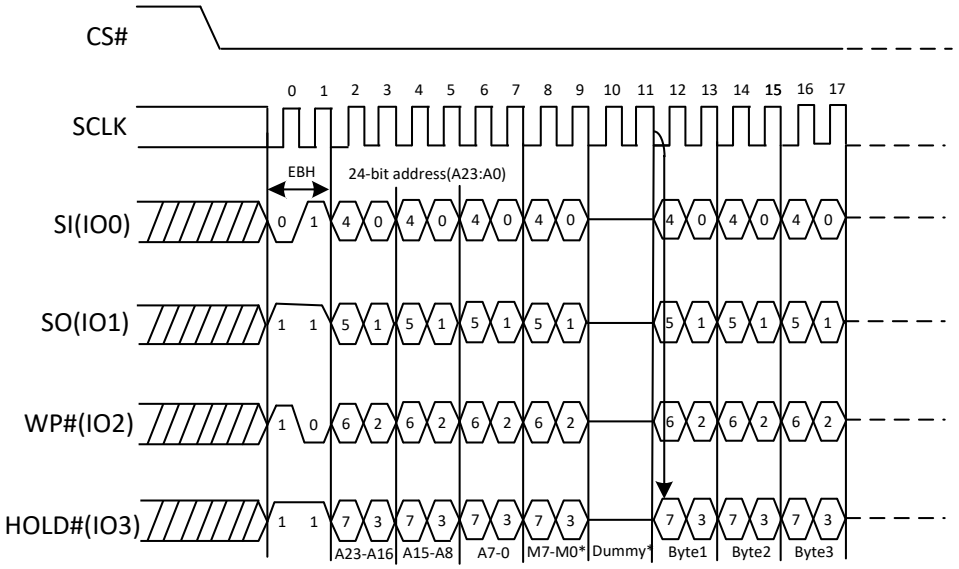
The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

Quad I/O Fast Read (EBH) in QPI mode

The Quad I/O Fast Read command is also supported in QPI mode. See the figure below. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8. In QPI mode, the "Continuous Read Mode" bits M7-M0 are also considered as dummy clocks. "Continuous Read Mode" feature is also available in QPI mode for Quad I/O Fast Read command. The "Wrap Around" feature is also available in QPI mode for Quad I/O Fast Read command. To use the "Wrap Around" Feature, the P2 in the "Set Read Parameters (C0H)" instruction in the QPI mode must be set to 0. To exit the "Wrap Around" Feature, the P2 in the "Set Read Parameters (C0H)" instruction in the QPI mode must be set to 1. The "Wrap Length" and the number of dummy clocks can be configured by the "Set Read Parameters (C0H)" instruction.

Figure 12b. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0) QPI)

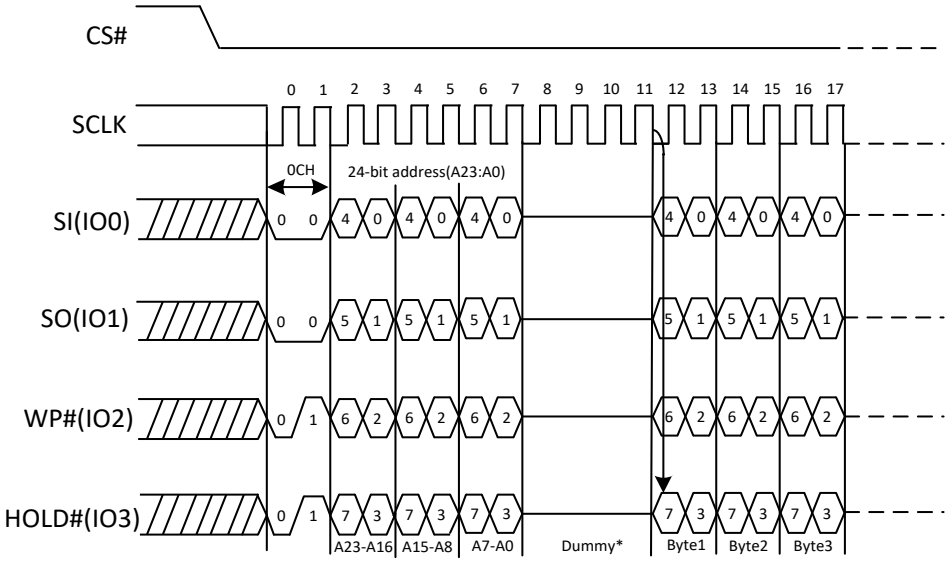


*Set Read Parameters Command (C0H) can set the number of dummy cycles

5.2.7. Burst Read With Wrap(0CH)

The “Burst Read with Wrap (0CH)” command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. This command is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command.

Figure 14. Burst Read with Wrap command Sequence Diagram



Note: The “Burst Read with Wrap (0CH)” instruction can always perform “Wrap Around” regardless of the Status of P2 in the “Set Read Parameters (C0H)” instruction in the QPI mode.

5.2.8. DTR Fast Read Quad I/O (EDH)

The DTR Fast Read Quad I/O (EDH) instruction is similar to the Fast Read Quad I/O (EBH) instruction except that address and data bits are input and output twice for each clock through four pins IO0, IO1, IO2 and IO3 and several Dummy clocks(including M7-M0) are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register must be set to enable the DTR Fast Read Quad I/O Instruction.

The number of dummy clocks for "DTR Fast Read Quad I/O" (EDH) can be set by the Latency Code (LC) in status register. When the LC bit is set to 0, which is default, the number of dummy clock cycles is 8. When the LC bit is set to 1, the number of dummy clock cycles is 6.

DTR Fast Read Quad I/O with "Continuous Read Mode"

The DTR Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in "6BH" command description. The upper nibble of the (M7-4) controls the length of the next DTR Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next DTR Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBH instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh/3FFh on IO0 for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 15. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10，SPI Mode)

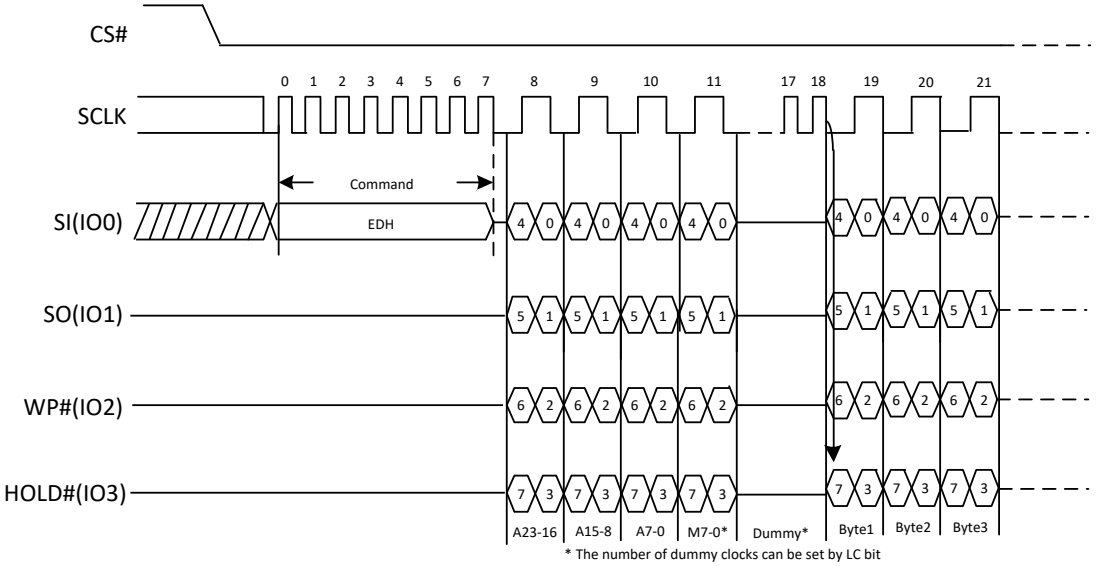
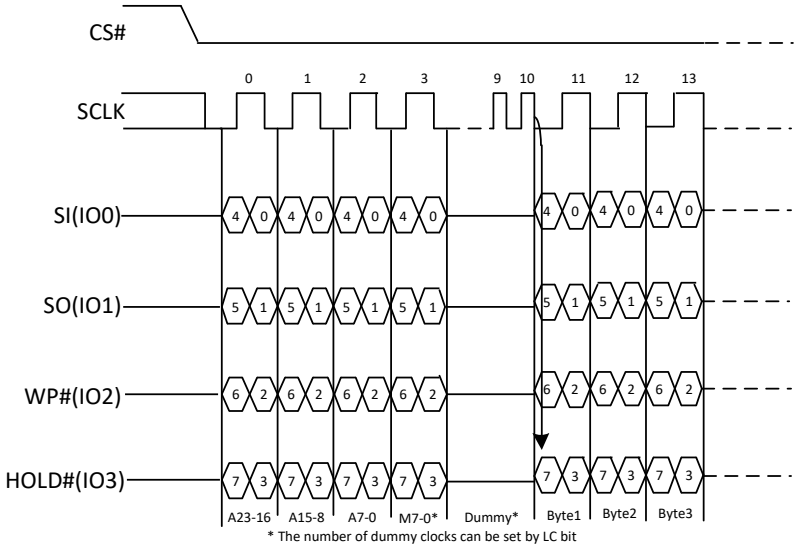


Figure 15a. DTR Fast Read Quad I/O (Previous instruction set M5-4=10，SPI Mode)



DTR Fast Read Quad I/O with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The DTR Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a “Set Burst with Wrap” (77H) command prior to EDH. The “Set Burst with Wrap” (77H) command can either enable or disable the “Wrap Around” feature for the following EDH commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

DTR Fast Read Quad I/O (EDH) in QPI Mode

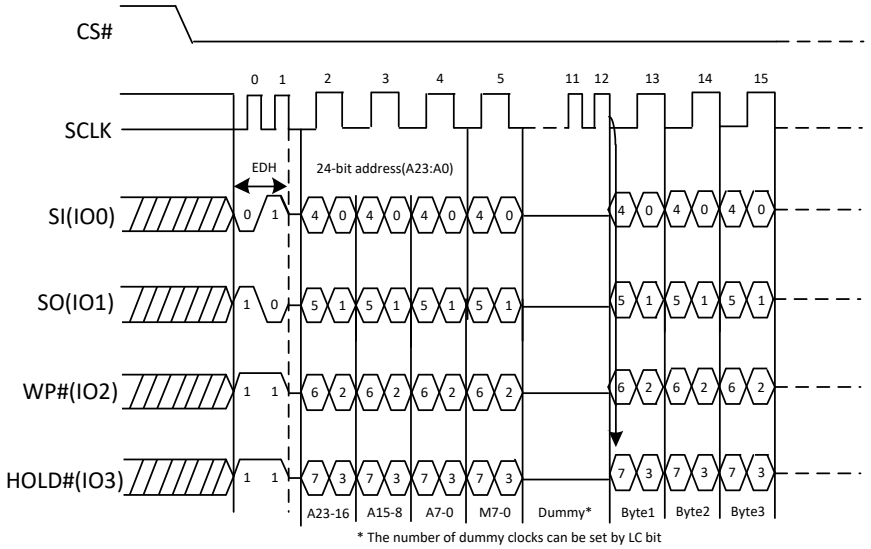
The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in the figure below. In QPI mode, the “Continuous Read Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

“Continuous Read Mode” feature is also available in QPI mode for DTR Fast Read Quad I/O instruction. Please refer to the description on previous pages.

The “Wrap Around” feature is also available in QPI mode for DTR Fast Read Quad I/O instruction. To use the “Wrap Around” Feature, the P2 in the “Set Read Parameters (C0H)” instruction in the QPI mode must be set to 0. To exit the “Wrap Around” Feature, the P2 in the “Set Read Parameters (C0H)” instruction in the QPI mode must be set to 1. The “Wrap Length” can be configured by the “Set Read Parameters (C0H)” instruction.

The number of dummy clocks for “DTR Fast Read Quad I/O” (EDH) can be set by the Latency Code (LC) in status register. When the LC bit is set to 0, which is default, the number of dummy clock cycles is 8. When the LC bit is set to 1, the number of dummy clock cycles is 6.

Figure 15b. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)



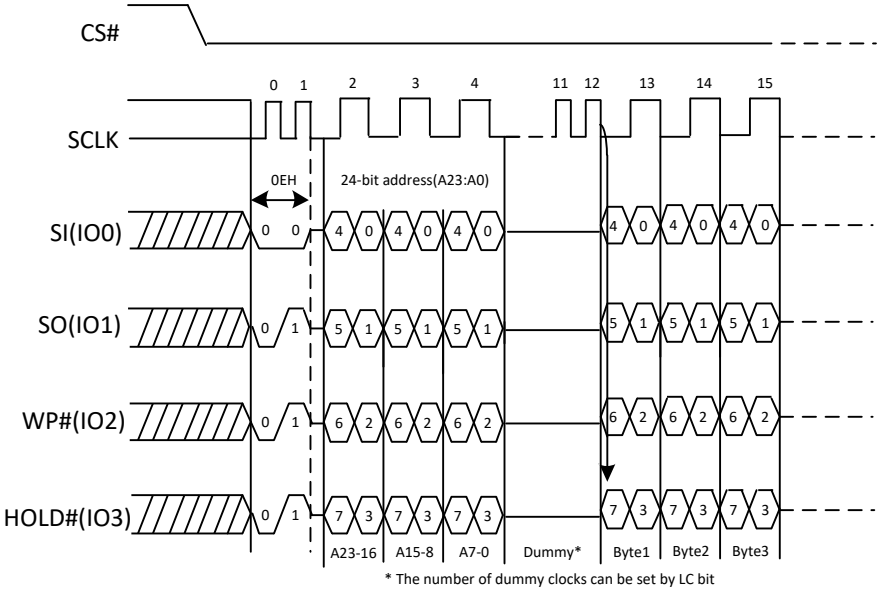
5.2.9. DTR Burst Read With Wrap(0EH)

The "DTR Burst Read with Wrap (0Eh)" instruction provides an alternative way to perform the read operation with "Wrap Around" in QPI mode. The instruction is similar to the "Fast Read (0Bh)" instruction in QPI mode, except the addressing of the read operation will "Wrap Around" to the beginning boundary of the "Wrap Length" once the ending boundary is reached.

The number of dummy clocks can be set by the Latency Code (LC) in status register. When the LC bit is set to 0, which is default, the number of dummy clock cycles is 8. When the LC bit is set to 1, the dummy clock cycles is 6.

The "Wrap Length" can be configured by the "Set Read Parameters (C0H)" instruction.

Figure 16. DTR Burst Read With Wrap command Sequence Diagram



Note: The "DTR Burst Read with Wrap (0EH)" instruction can always perform "Wrap Around" regardless of the Status of P2 in the "Set Read Parameters (C0H)" instruction in the QPI mode.

5.2.10. Page Program(02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low →sending Page Program command→ 3-byte address on SI→ at least 1 byte data on SI →CS# goes high. The command sequence is shown in Figure 17. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.

Figure 17. Page Program Sequence Diagram

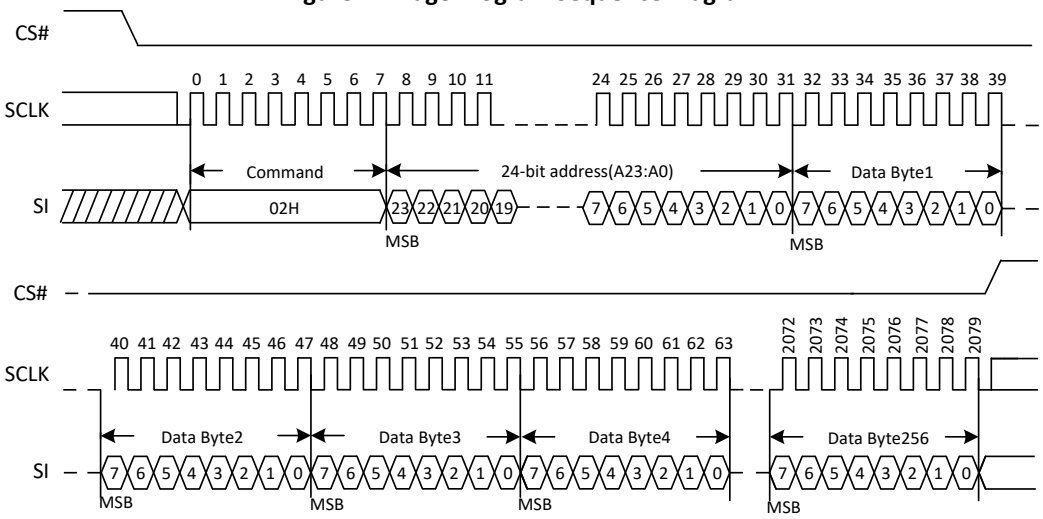
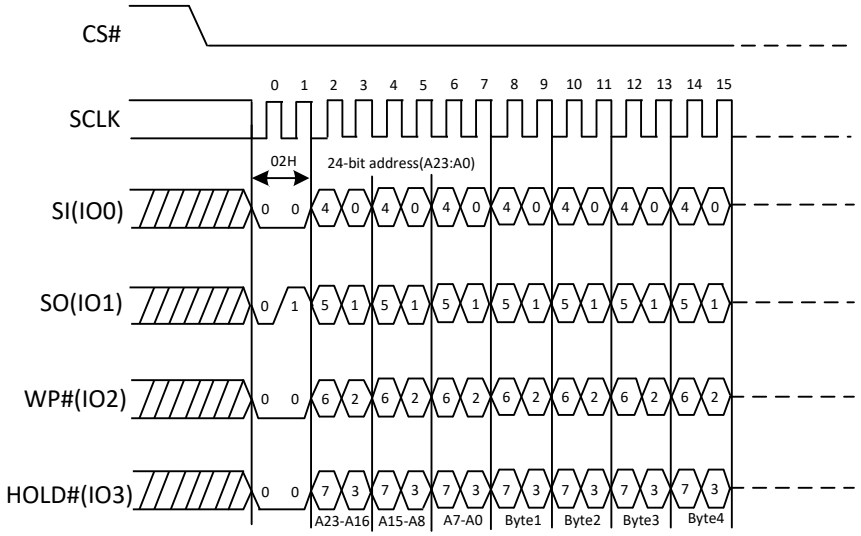


Figure 17a. Page Program Sequence Diagram (QPI)



5.2.11. Quad Page Program(32H)

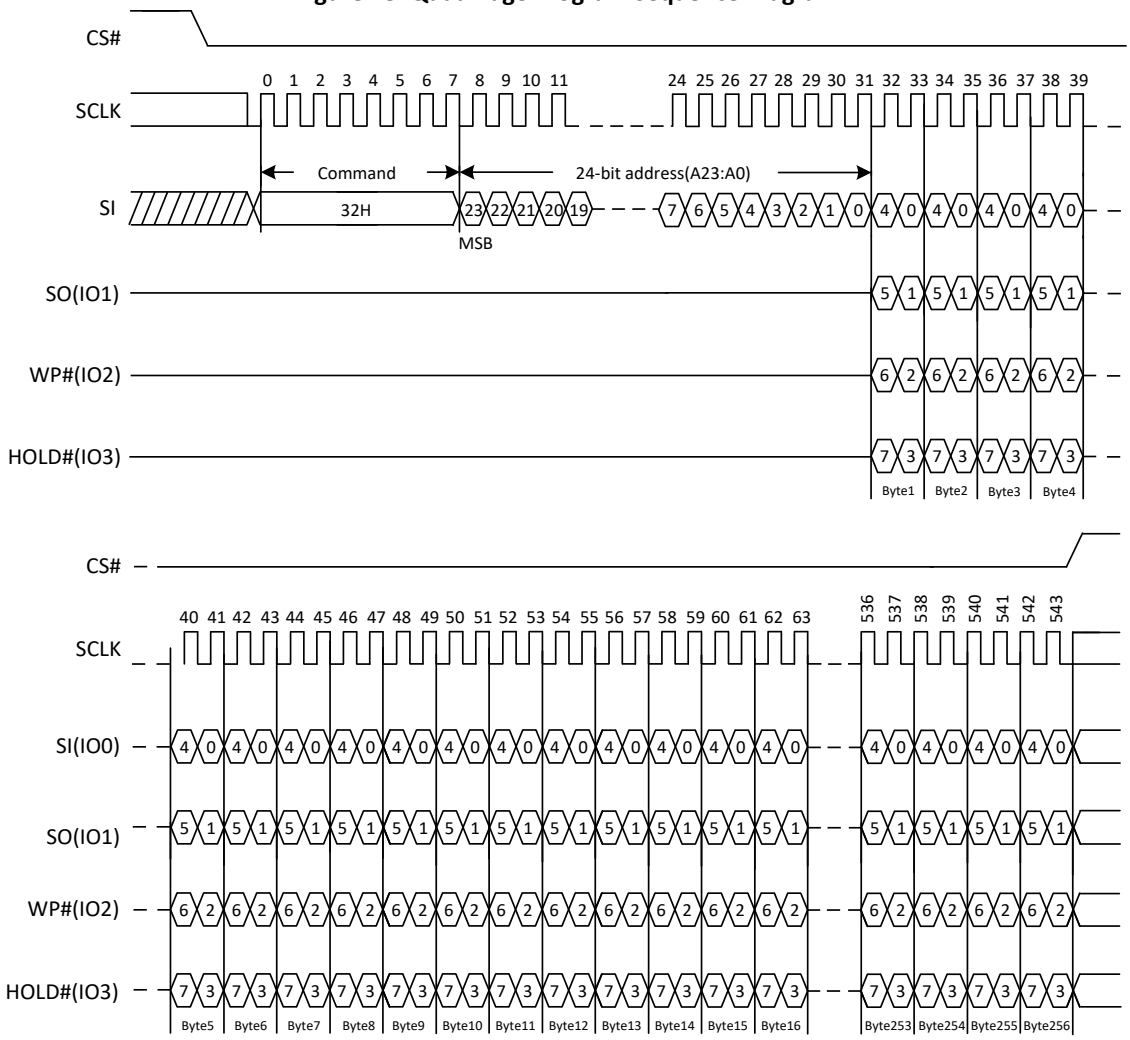
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program, the Quad Enable bit in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The Quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in the figure below. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command will not be executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) will not be executed.

Figure 18. Quad Page Program Sequence Diagram



5.2.12. Extend Quad Page Program (C2H)

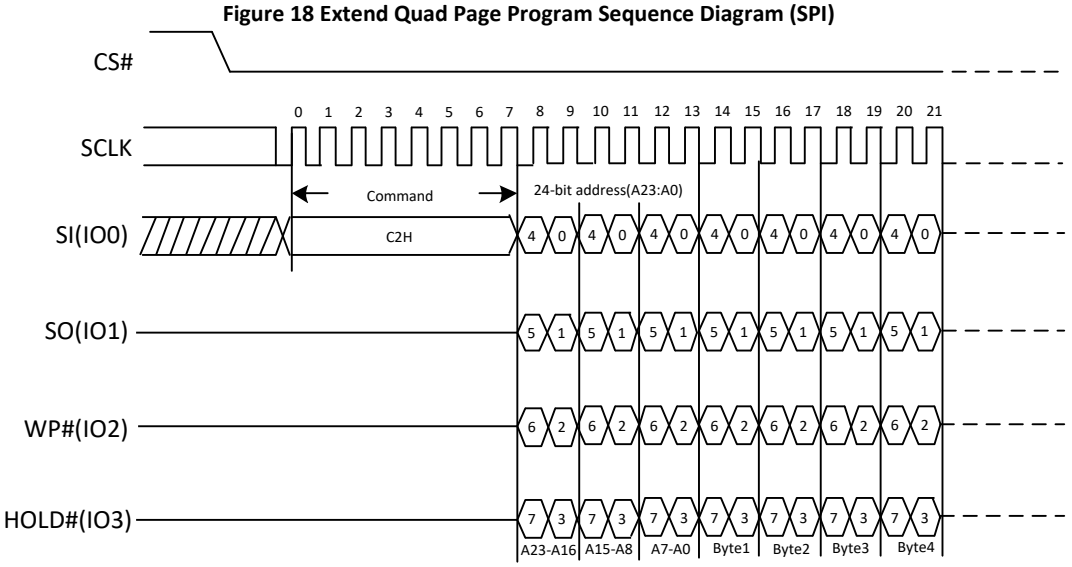
The Extend Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The extend quad Page Program command is entered by driving CS# Low, followed by the command code (C2H), three address bytes and at least one data byte on IO pins.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Extend Quad Page Program (EPP) command is not executed.

As soon as CS# is driven high, the self-timed Extend Quad Page Program cycle (whose duration is tPP) is initiated. While the Extend Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Extend Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

An Extend Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 18 Extend Quad Page Program Sequence Diagram (SPI)



5.2.13. Sector Erase(20H)

The Sector Erase (SE) command is for erasing all the data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Sector Erase command. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command.

The Sector Erase command sequence: CS# goes low→ sending Sector Erase command→ 3-byte address on SI→ CS# goes high. The command sequence is shown in Figure 19. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command will not be executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit (see Table 1.0 & 1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 19. Sector Erase Sequence Diagram

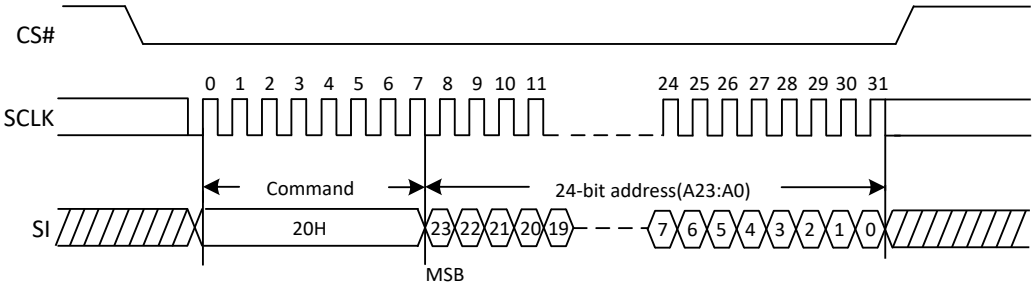
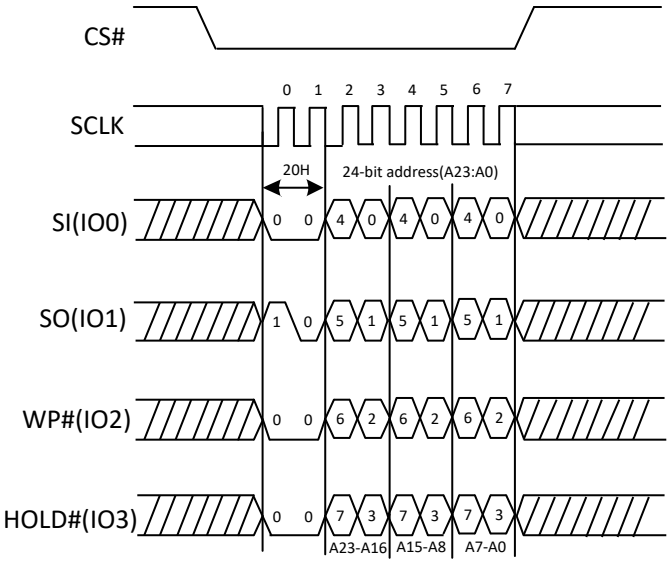


Figure 19a. Sector Erase Sequence Diagram (QPI)



5.2.14. 32k Block Erase(52H)

The 32KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the 32KB Block Erase command. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI, driving CS# high. Any address inside the block is a valid address for the 32KB Block Erase (BE) command.

The 32KB Block Erase command sequence: CS# goes low→ sending 32KB Block Erase command→ 3-byte address on SI→CS# goes high. The command sequence is shown in Figure 20. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.0 & 1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 20. 32KB Block Erase Sequence Diagram

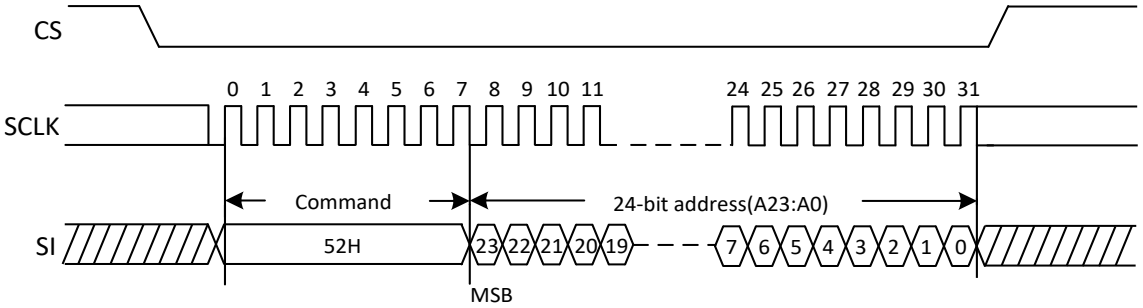
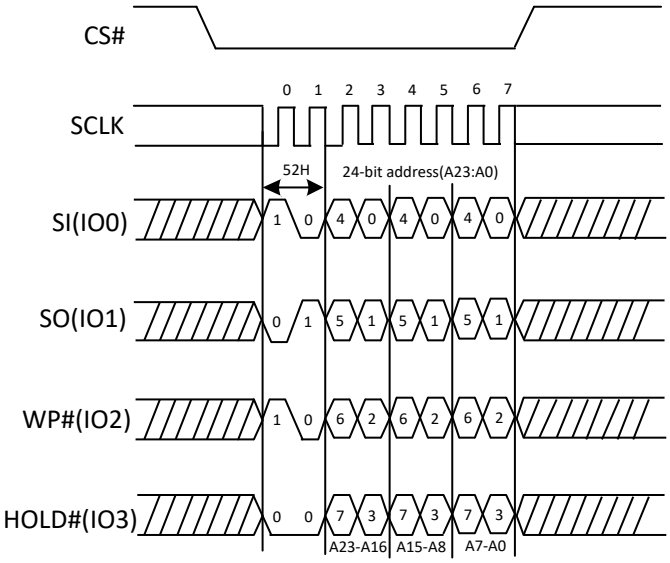


Figure 20a. 32KB Block Erase Sequence Diagram (QPI)



5.2.15. 64k Block Erase(D8H)

The 64KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the 64KB Block Erase command. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI, driving CS# high. Any address inside the block is a valid address for the 64KB Block Erase (BE) command.

The 64KB Block Erase command sequence: CS# goes low →sending 64KB Block Erase command→ 3-byte address on SI→CS# goes high. The command sequence is shown in Figure 21. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table 1.0 & 1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 21. 64KB Block Erase Sequence Diagram

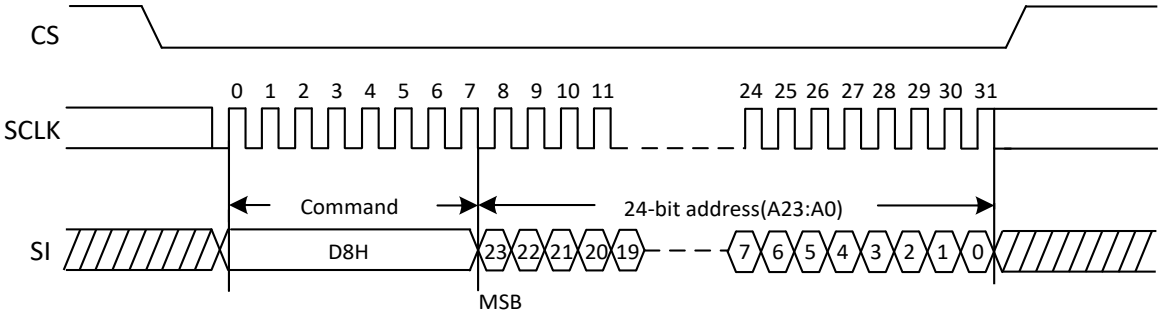
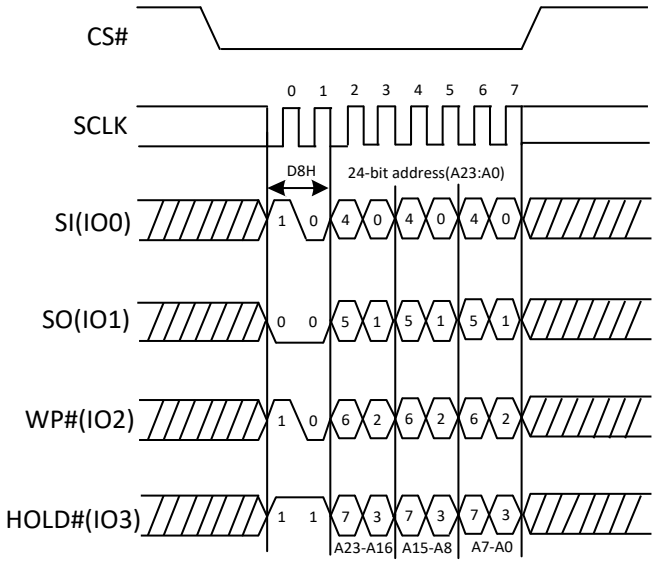


Figure 21a. 64KB Block Erase Sequence Diagram (QPI)



5.2.16. Chip Erase(60H or C7H)

The Chip Erase (CE) command is for erasing all the data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the Chip Erase command .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI).

The Chip Erase command sequence: CS# goes low→ sending Chip Erase command→CS# goes high. The command sequence is shown in Figure 22. CS# must be driven high after the eighth bit of the command code has been latch in, otherwise the Chip Erase command will not be executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 22. Chip Erase Sequence Diagram

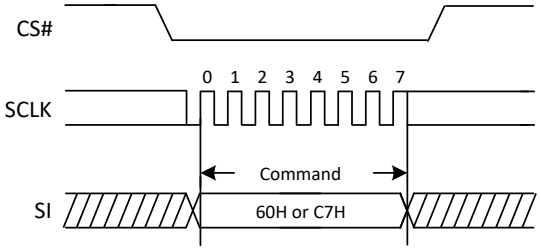
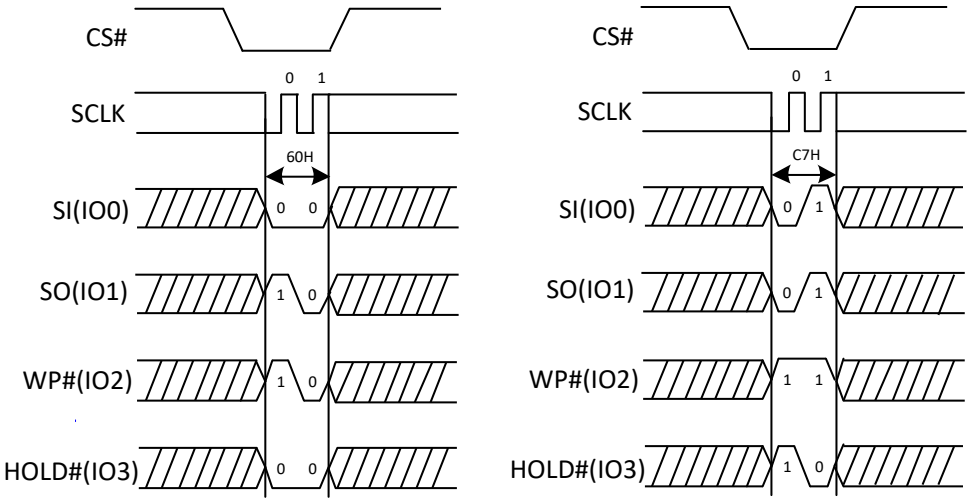


Figure 22a. Chip Erase Sequence Diagram (QPI)



5.3. Device Operations

5.3.1. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Read Parameter setting (P7-P0) and Wrap Bit Setting (W6-W4).

The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST_R to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

The Enable Reset (66H) command must be issued prior to a Reset(99H) command and any other commands can't be inserted between them. Otherwise, Enable Reset (66H) command will be cleared.

Figure 23. Enable Reset and Reset command Sequence Diagram

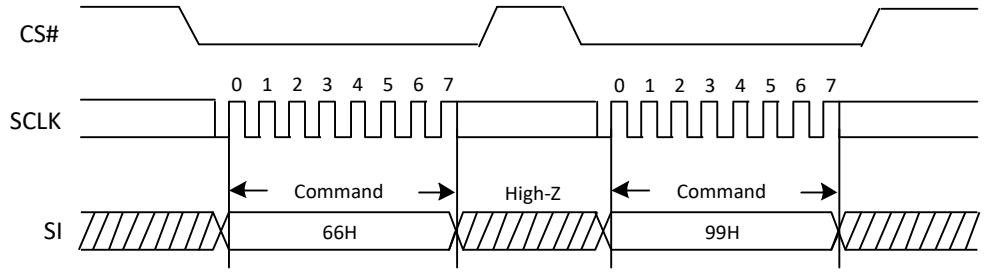
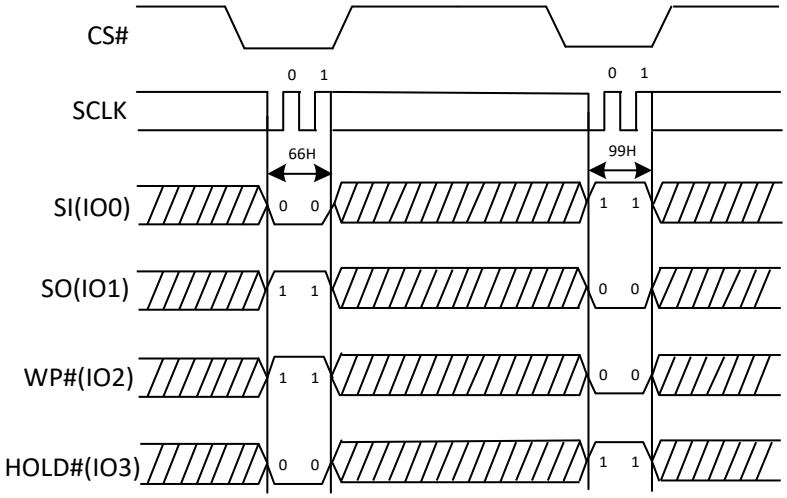


Figure 23a. Enable Reset and Reset command Sequence Diagram (QPI)



5.3.2. Write Enable(06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Erase Security Register, Program Security Register and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low -> Sending the Write Enable command -> CS# goes high.

Figure 24.Write Enable Sequence Diagram

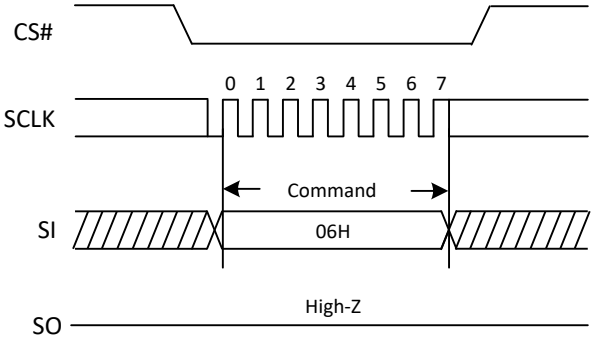
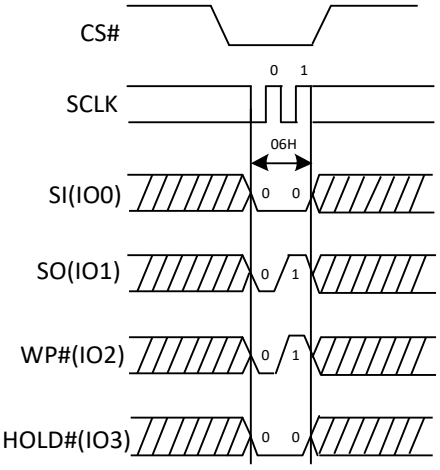


Figure 24a. Write Enable Sequence Diagram (QPI)



5.3.3. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure 25.Write Enable for Volatile Status Register Sequence Diagram

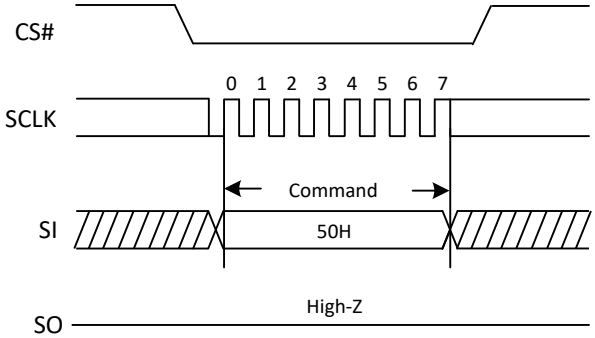
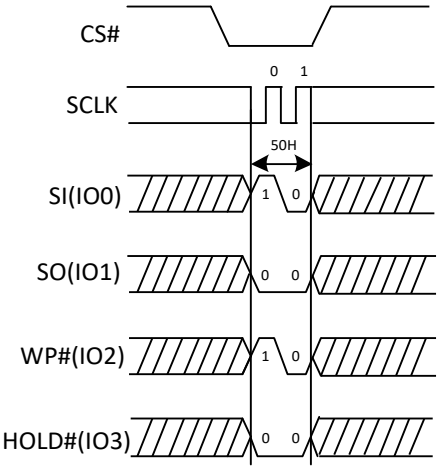


Figure 25a. Write Enable for Volatile Status Register Sequence Diagram (QPI)



5.3.4. Write Disable(04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low ->Sending the Write Disable command ->CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

Figure 26. Write Disable Sequence Diagram

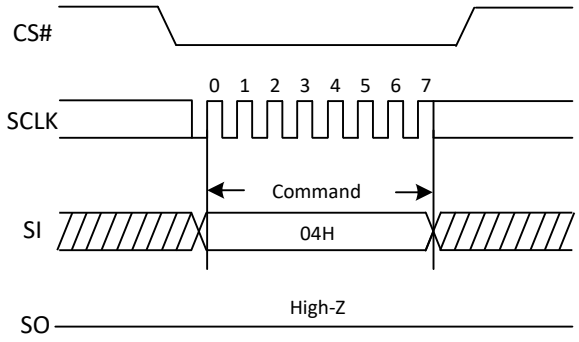
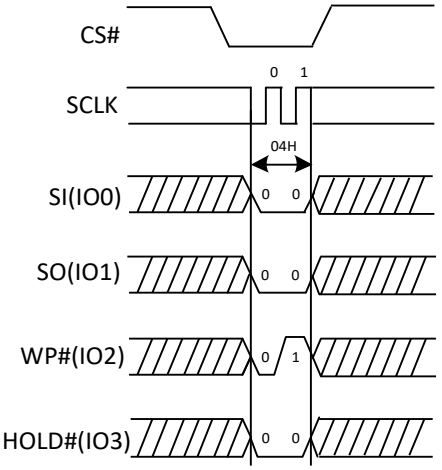


Figure 26a. Write Disable Sequence Diagram (QPI)



5.3.5. Program Erase Suspend(75H)

The Program/Erase Suspend command “75H”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H/31H/11H) and Erase/Program Security Registers command (44H,42H) and Erase commands (20H, 52H, D8H, C7H, 60H) and Page Program command (02H / 32H) are not allowed during Program suspend. The Write Status Register command (01H/31H/11H) and Erase Security Registers command (44H) and Erase commands (20H, 52H, D8H, C7H, 60H) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tSUS” (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared form 1 to 0 within “tSUS” and the SUS bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state. The command sequence is show in Figure 27.

Figure 27. Program/Erase Suspend Sequence Diagram

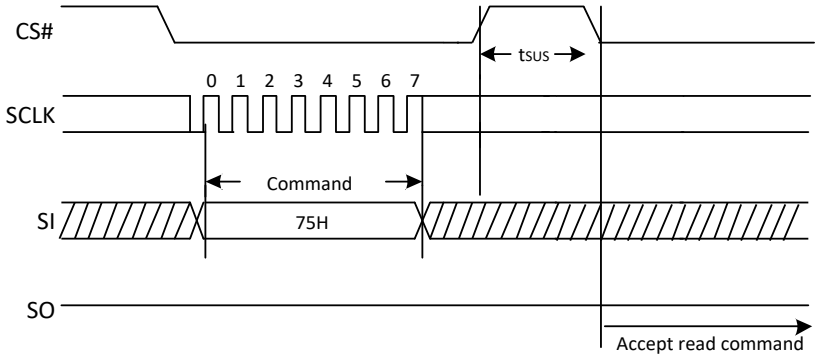
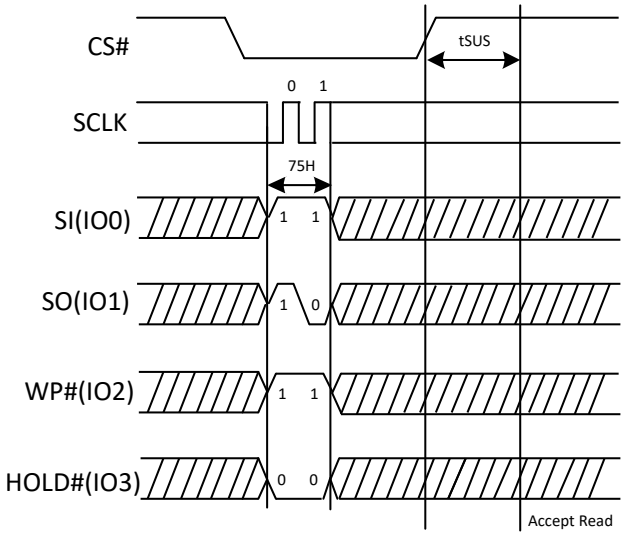


Figure 27a. Program/Erase Suspend Sequence Diagram(QPI)



5.3.6. Program Erase Resume (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase command will be accepted by the device only if the SUS bit equal to 1 and the WIP bit equal to 0. After issued the SUS bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active. The command sequence is show in Figure 28.

Figure 28. Program/Erase Resume Sequence Diagram

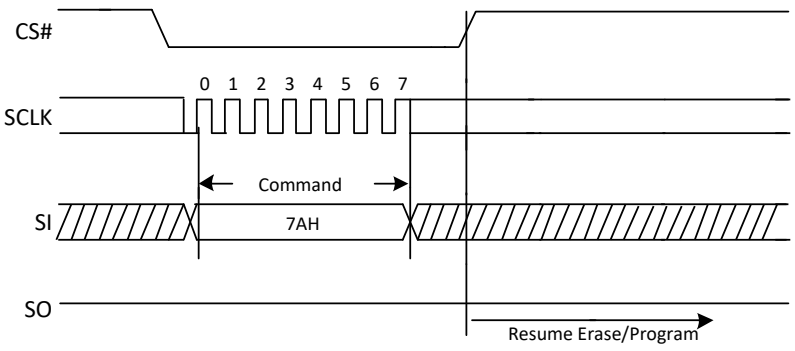
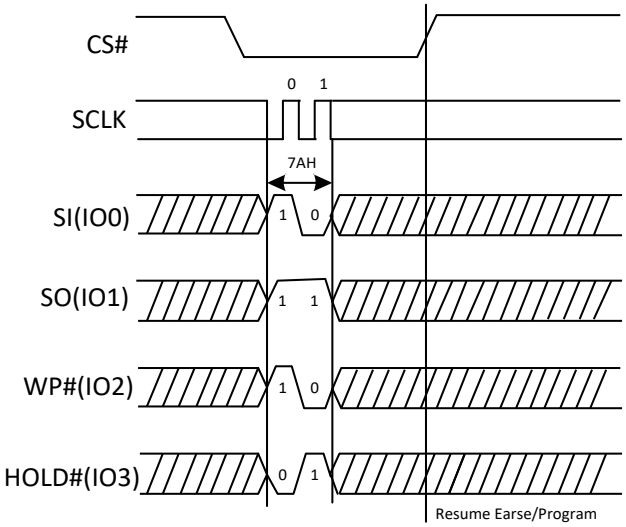


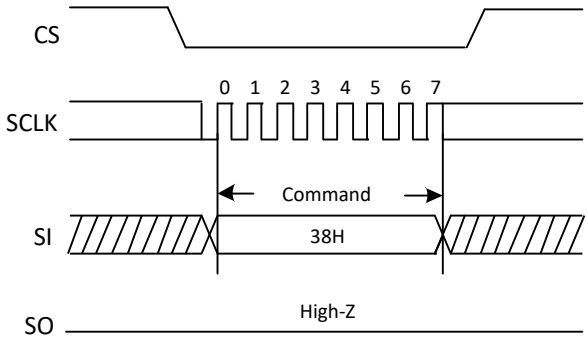
Figure 28a. Program/Erase Resume Sequence Diagram (QPI)



5.3.7. Enable QPI(38H)

The device support both Standard/Dual/Quad SPI and QPI mode. The "Enable QPI (38H)" command can switch the device from SPI mode to QPI mode. See the command Table 2 for all support QPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register must be set to 1 first, and "Enable QPI (38H)" command must be issued. If the QE bit is 0, the "Enable QPI (38H)" command will be ignored and the device will remain in SPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged.

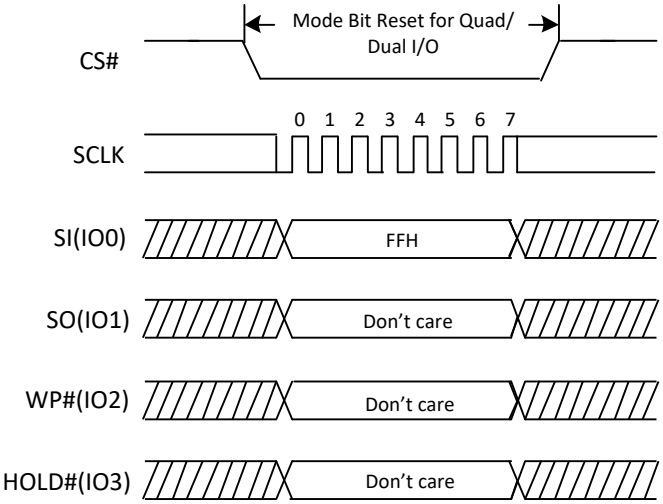
Figure 29. Enable QPI mode command Sequence Diagram



5.3.8. Continuous Read Mode Reset / Disable QPI (FFH)

The Dual/Quad I/O Fast Read operations, “Continuous Read Mode” bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to “AXH”, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH /EDH command code. If Continuous Read Mode bits are set to “AXH”, the device will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the “AXH” state and allow standard SPI command to be recognized.

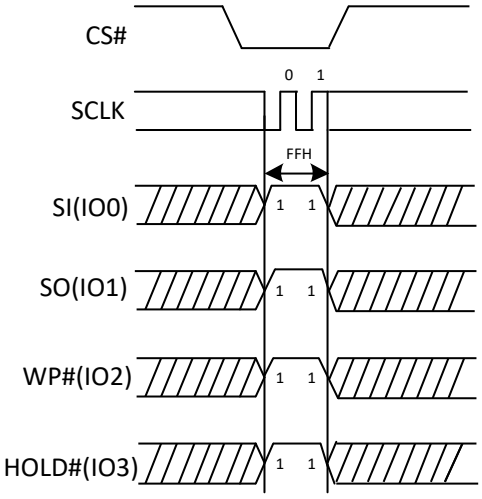
Figure 30. Continuous Read Mode Reset Sequence Diagram



Disable QPI (FFH)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, the “Disable QPI (FFH)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged. When the device is in QPI mode, the first FFH command will exit continuous read mode and the second FFH command will exit QPI mode.

Figure 30a. Disable QPI mode command Sequence Diagram



5.3.9. Set Burst With Wrap(77H)

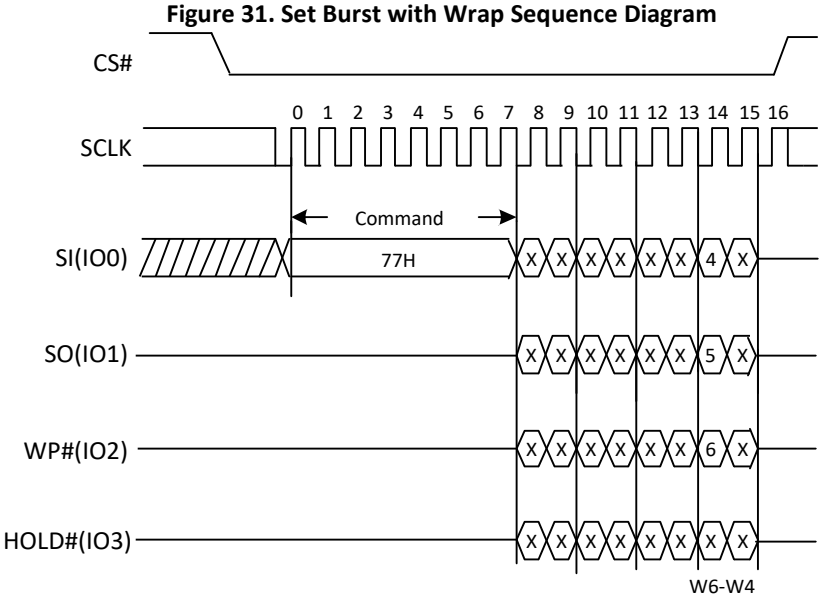
The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read (EBH)", and "Quad Read under DTR (EDH)" commands to access a fixed length of 8/16/32/64-byte section within a 256-byte page in standard SPI mode. The Set Burst with Wrap command sequence: CS# goes low →Send Set Burst with Wrap command →Send 24 dummy bits →Send 8 bits "Wrap bits"→CS# goes high

W6,W5	W4=0		W4=1(default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0,0	Yes	8-byte	No	N/A
0,1	Yes	16-byte	No	N/A
1,0	Yes	32-byte	No	N/A
1,1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read (EBH)" and "Quad Read under DTR (EDH)" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

In QPI mode, the "Burst Read with Wrap (0CH)" command should be used to perform the Read Operation with "Wrap Around" feature. The Wrap Length set by W5-W6 in Standard SPI mode is still valid in QPI mode and can also be re-configured by "Set Read Parameters (C0H) command, and vice versa.

Figure 31. Set Burst with Wrap Sequence Diagram



5.3.10. Set Read Parameters(C0H)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read-frequency or minimum data access latency, “Set Read Parameters (C0H)” instruction can be used to configure the number of dummy clocks for “Fast Read (0BH)”, “Fast Read Quad I/O (EBH)” , “Burst Read with Wrap (0CH)” , “Read SFDP (5AH)” , “Read Unique ID (4BH)” , “Read Security Register (48H)” and “Release From Deep Power-Down And Read Device ID (ABH)” instructions, and to configure the number of bytes of “Wrap Length” for “Fast Read Quad I/O (EBH)”, “DTR Fast Read Quad I/O (EDH)”, “DTR Burst Read with Wrap (0EH)” and “Burst Read with Wrap (0CH)” instruction. In Standard SPI mode, the “Set Read Parameters (C0H)” instruction is not accepted.

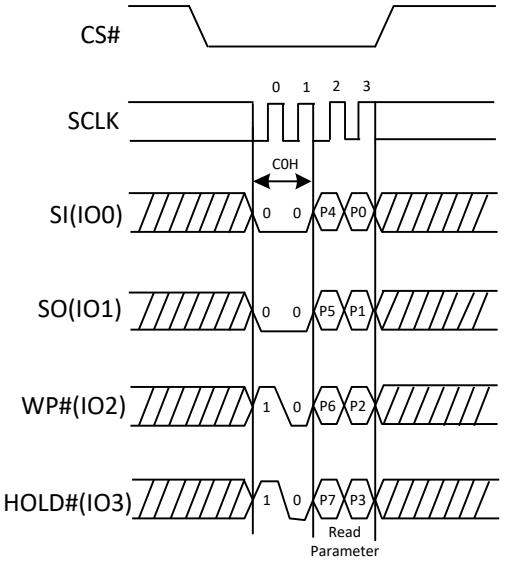
The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed and will remain unchanged when the device is switched from Standard SPI mode to QPI mode and requires to be set again, prior to any 0BH or EBH instructions. When the device is switched from QPI mode to SPI mode, the number of dummy clocks goes back to default.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 8. The “Wrap Length” is set by W6-4 bit in the “Set Burst with Wrap (77H)” instruction in Standard SPI mode and by P1-P0 in the “Set Read Parameters (C0H)” in the QPI mode. The Wrap Length set by P1-P0 in QPI mode is still valid in SPI mode and can also be re-configured by “Set Burst with Wrap (77H)”, and vice versa.

C0H adds an extra bit P2 for Disable/Enable Wrap function. Execute C0H and then follows EBH or EDH, performs the read operation with “Wrap Around” in QPI mode. This function is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command. Also 0CH and 0EH are alternative ways to perform “Wrap Around”, they can always perform “Wrap Around” regardless of the Status of P2 in the “Set Read Parameters (C0H)” instruction in the QPI mode.

P5-P4	Dummy Clocks	Maximum Read Freq.	P2	P1-P0	Wrap Length
0 0	4	70MHz	Enable Wrap=0	0 0(Default)	8-byte
0 1	4	70MHz	Disable Wrap=1 (Default)	0 1	16-byte
1 0	6	108MHz		1 0	32-byte
1 1 (Default)	8	108MHz		1 1	64-byte

Figure 31. Set Read Parameters command Sequence Diagram



5.3.11. Deep Power-Down(B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest power consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But the Standby Mode is different from the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the flash memory has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID command (ABH) and software reset (66H+99H). This command releases the flash memory from the Deep Power-Down Mode.

The Deep Power-Down Mode automatically stops at Power-Off, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI, driving CS# high.

The Deep Power-Down command sequence: CS# goes low→sending Deep Power-Down command→CS# goes high. The command sequence is shown in Figure 32. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command will not be executed. As soon as CS# is driven high, it requires a time duration of tDP before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any input of Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 32. Deep Power-Down Sequence Diagram

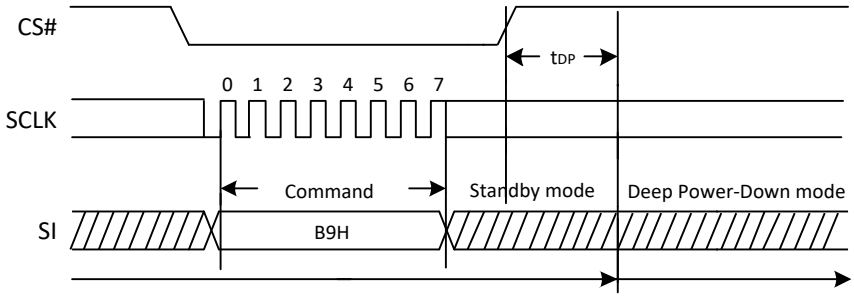
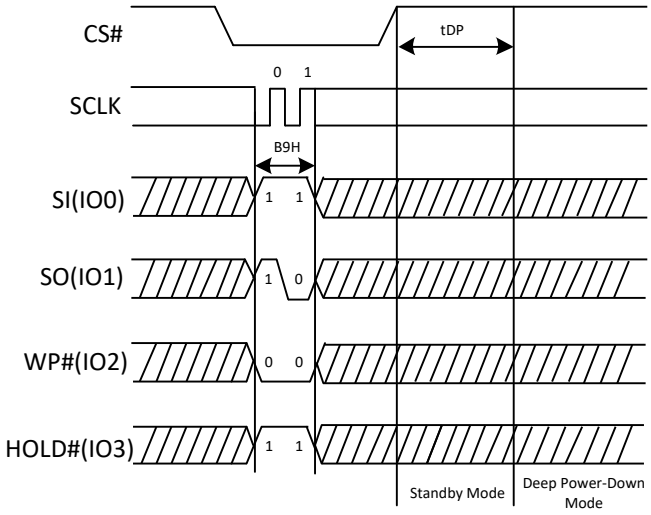


Figure 32a. Deep Power-Down Sequence Diagram (QPI)



5.3.12. Release From Deep Power-Down(ABH)

The Release from Deep Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from Deep Power-Down Mode or obtain the devices electronic identification (ID) number.

To release the device from Deep Power-Down Mode, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown in Figure 33. Release from Deep Power-Down Mode will take the time duration of tRES1 (See AC Characteristics) before the device resume to normal state and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When the command is used only to obtain the Device ID while the flash memory is not in Deep Power-Down Mode, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 33b. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When the command is used to release the device from Deep Power-Down Mode and obtain the Device ID, the command is the same as previously described, and shown in Figure 33b. , except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume to normal mode and other command will be accepted. If the Release from Deep Power-Down and Read Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command will be ignored and will not affect the current cycle.

Figure 33. Release Power-Down Sequence Diagram

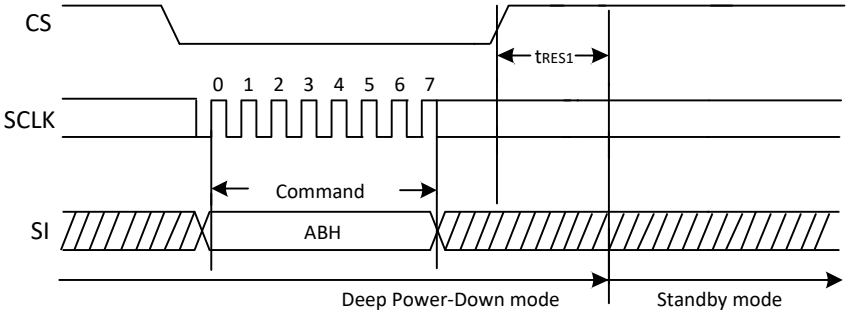


Figure 33a. Release Power-Down Sequence Diagram (QPI)

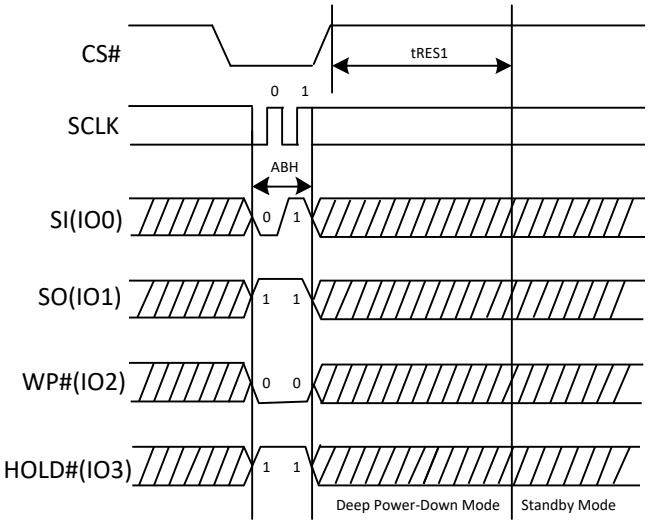
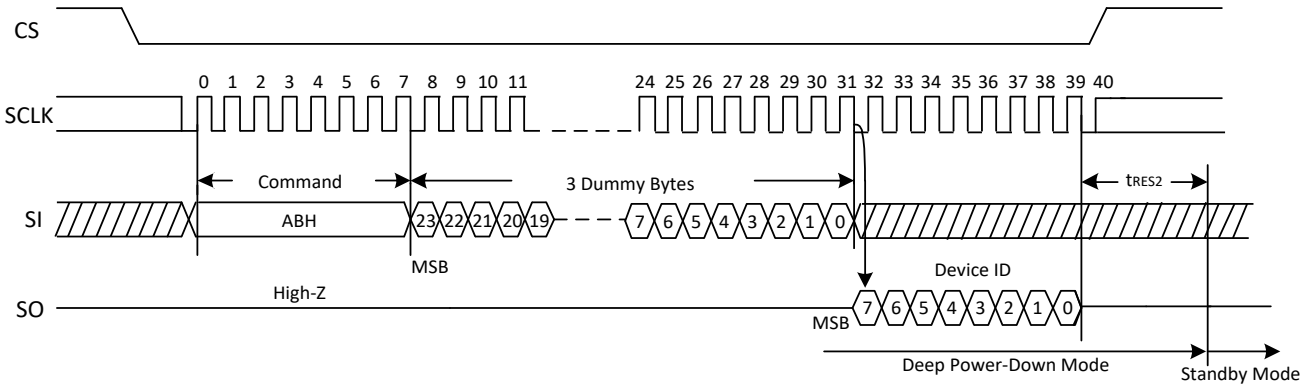


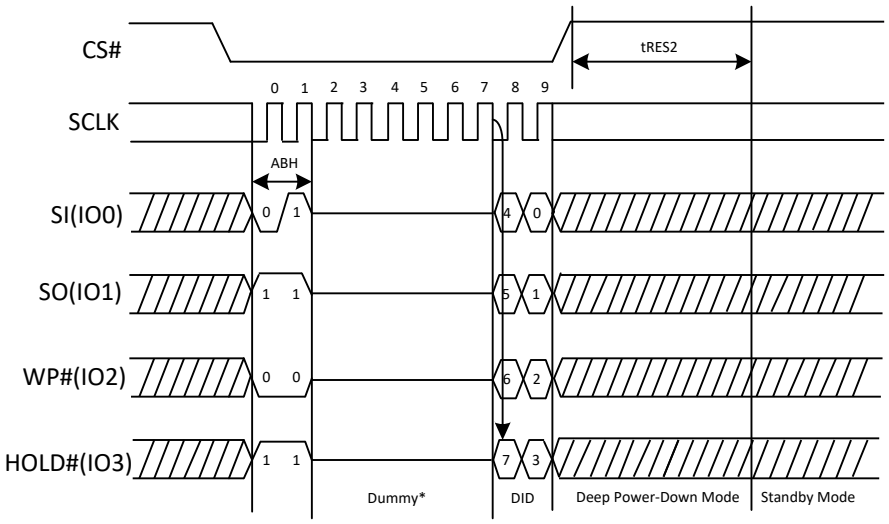
Figure 33b. Release Power-Down/Read Device ID Sequence Diagram



Release From Deep Power-Down/Read Device ID (ABH) in QPI mode

The Release From Deep Power-Down/Read Device ID command is also supported in QPI mode. See the figure below, In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Figure 33c. Release Power-Down/Read Device ID Sequence Diagram (QPI)



*Set Read Parameters Command (C0H) can set the number of dummy cycles

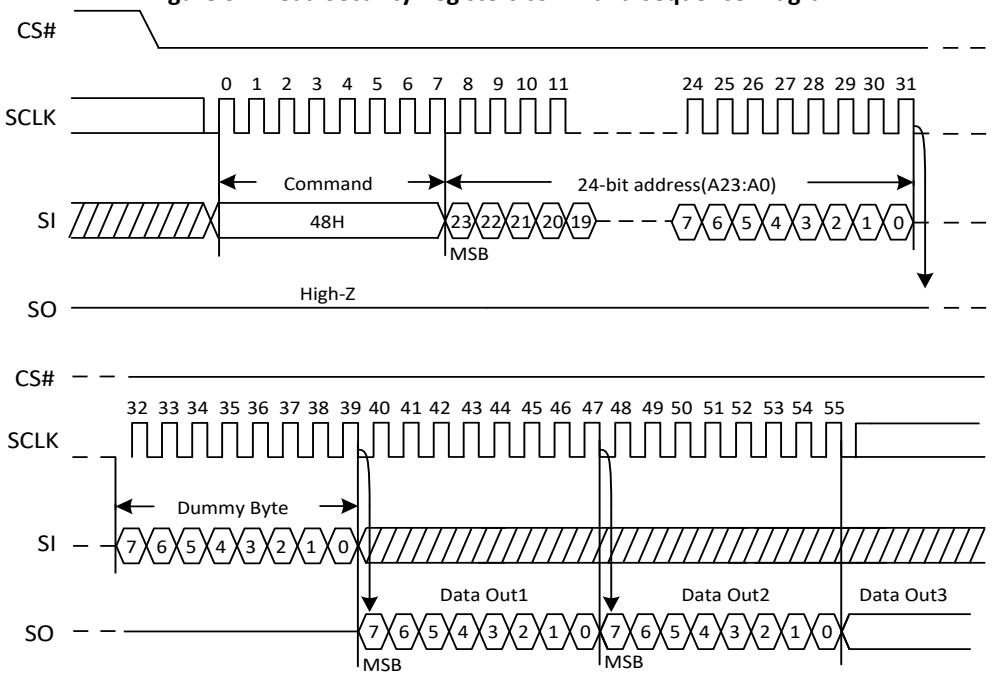
5.4. One-Time Programmable (OTP) Operations

5.4.1. Read Security Register(48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-A16	A15-A12	A11-A10	A9-A0
Security Registers #1	00000000	0001b	00b	Byte Address
Security Registers #2	00000000	0010b	00b	Byte Address
Security Registers #3	00000000	0011b	00b	Byte Address

Figure 34. Read Security Registers command Sequence Diagram

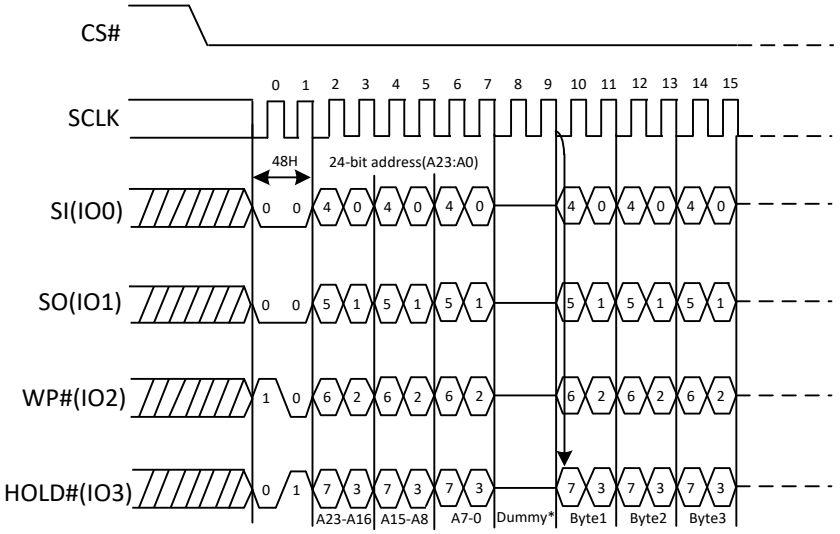


Note: The Byte Address A2-A0 must be 000.

Read Security Register (48H) in QPI mode

The Read Security Register command is also supported in QPI mode. See the figure below, In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Figure 34a. Read Security Registers command Sequence Diagram (QPI)



*Set Read Parameters Command (C0H) can set the number of dummy cycles

5.4.2. Program Security Register(42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 1024 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB1, LB2, LB3) is set to 1, the corresponding Security Registers (#1, #2, #3) will be permanently locked. Program Security Registers command will be ignored.

Address	A23-A16	A15-A12	A11-A10	A9-A0
Security Registers #1	00000000	0001b	00b	Byte Address
Security Registers #2	00000000	0010b	00b	Byte Address
Security Registers #3	00000000	0011b	00b	Byte Address

Figure 35. Program Security Registers command Sequence Diagram

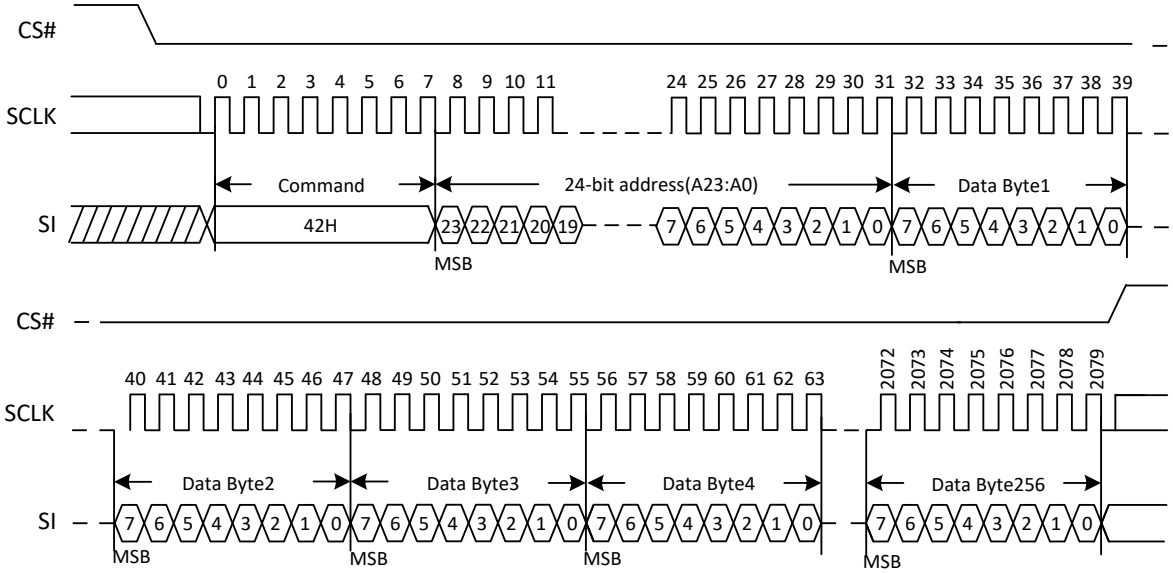
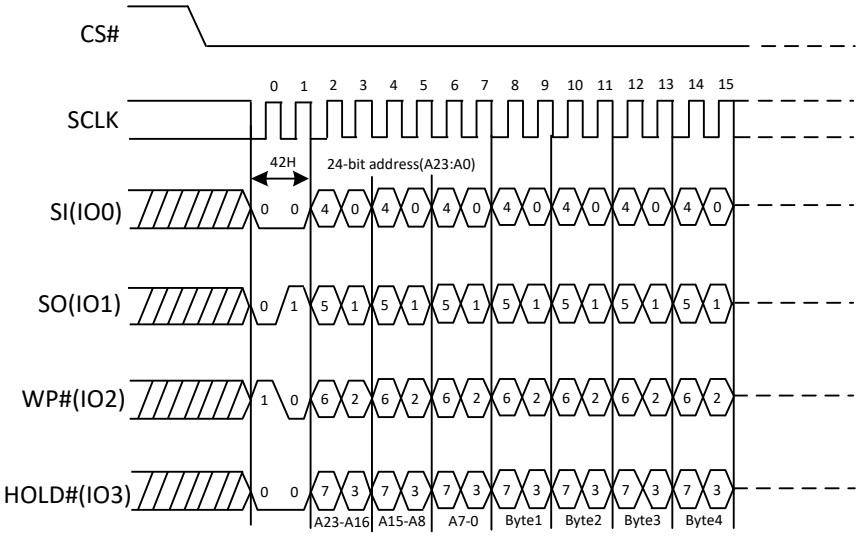


Figure 35a. Program Security Registers command Sequence Diagram (QPI)



5.4.3. Erase Security Register(44H)

The device provides 3x1024-byte Security Registers which only erased each 1024-byte at once. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low -> sending Erase Security Registers Command -> CS# goes high. The command sequence is shown in Figure 36. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB1, LB2, LB3) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the corresponding Security Registers (#1, #2, #3) will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-A16	A15-A12	A11-A10	A9-A0
Security Registers #1	00000000	0001b	00b	Don't Care
Security Registers #2	00000000	0010b	00b	Don't Care
Security Registers #3	00000000	0011b	00b	Don't Care

Figure 36. Erase Security Registers command Sequence Diagram

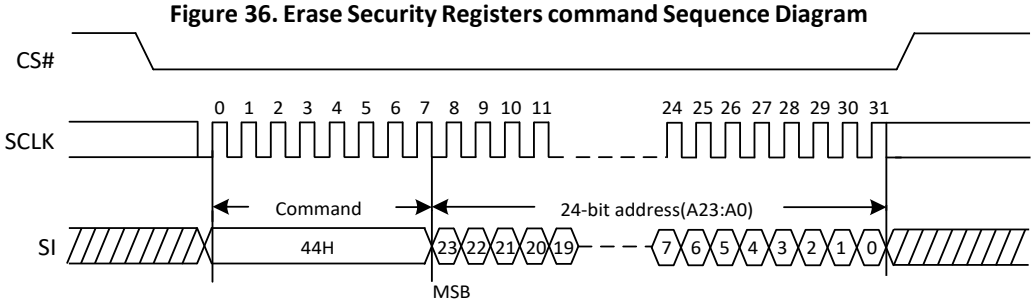
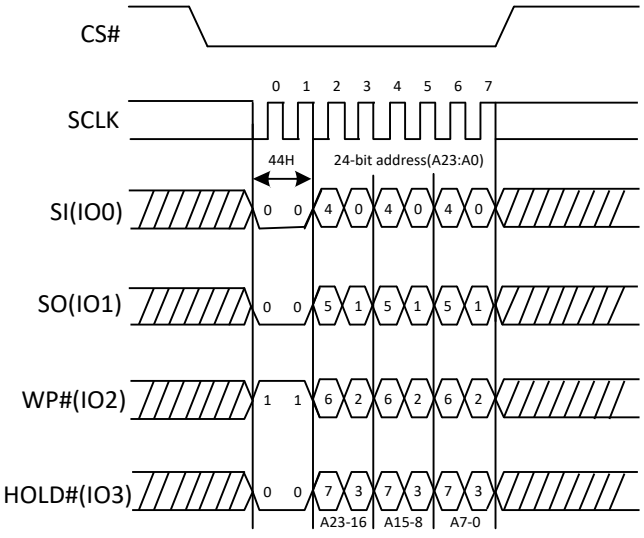


Figure 36a. Erase Security Registers command Sequence Diagram



5.5. Advanced Data Protection

5.5.1. Global Block/Sector Lock (7EH) or Unlock (98H)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock command, or can set to 0 by the Global Block/Sector Unlock command.

The Global Block/Sector Lock command (7EH) sequence: CS# goes low –> SI: Sending Global Block/Sector Lock command –> CS# goes high. The command sequence is shown in Figure 37.

The Global Block/Sector Unlock command (98H) sequence: CS# goes low –> SI: Sending Global Block/Sector Unlock command –> CS# goes high. The command sequence is shown in Figure 37b.

Figure 37. The Global Block/Sector Lock Sequence Diagram

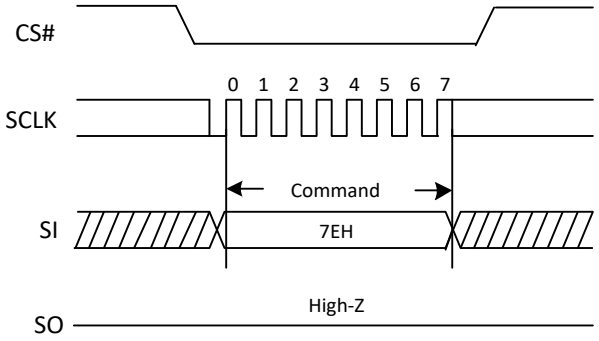


Figure37a. The Global Block/Sector Lock Sequence Diagram (QPI)

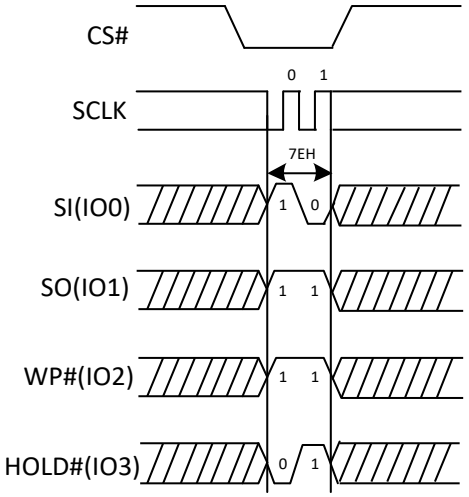


Figure 37b. The Global Block/Sector Unlock Sequence Diagram

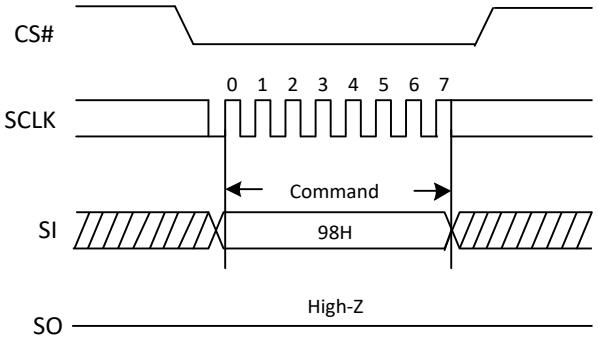
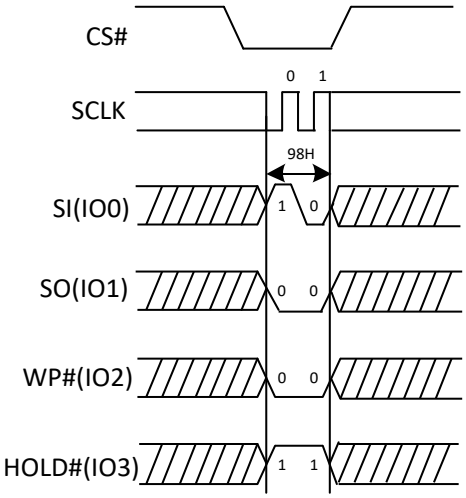


Figure 37c. The Global Block/Sector Unlock Sequence Diagram (QPI)



5.5.2. Individual Block/Sector Lock (36H) / Unlock (39H) / Read (3DH)

The individual block/sector lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, BP (4:0) bits in the Status Register. The Individual Block/Sector Lock bits are volatile bits, the default values of which after device power up or after a Reset are 1.

The individual Block/Sector Lock command (36H) sequence: CS# goes low –> SI: Sending individual Block/Sector Lock command –> SI: Sending 24bits individual Block/Sector Lock Address –> CS# goes high. The command sequence is shown in Figure 38.

The individual Block/Sector Unlock command (39H) sequence: CS# goes low –> SI: Sending individual Block/Sector Unlock command –> SI: Sending 24bits individual Block/Sector Lock Address –> CS# goes high. The command sequence is shown in Figure 38a.

The Read individual Block/Sector lock command (3DH) sequence: CS# goes low –> SI: Sending Read individual Block/Sector Lock command –> SI: Sending 24bits individual Block/Sector Lock Address –> SO: The Block/Sector Lock Bit will out –> CS# goes high. If the least significant bit(LSB) is1, the corresponding block/sector is locked, if the LSB is 0, the corresponding block/sector is unlocked, Erase/Program operation can be performed. The command sequence is shown in Figure 38c.

Figure 38. Individual Block/Sector Lock command Sequence Diagram

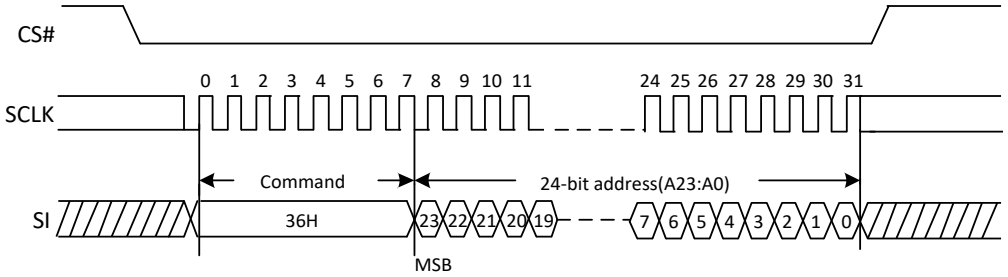


Figure 38a. Individual Block/Sector Lock command Sequence Diagram (QPI)

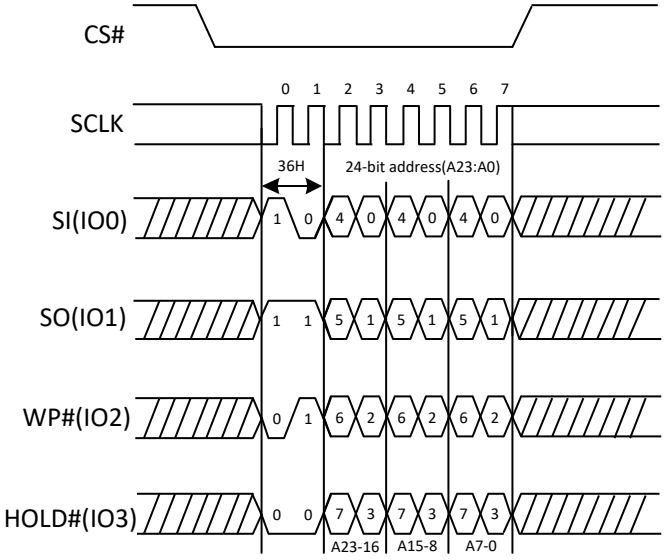


Figure 38b. Individual Block/Sector Unlock command Sequence Diagram

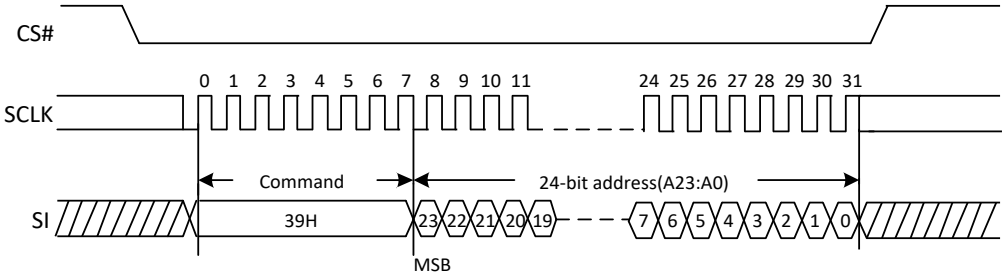


Figure 38c. Individual Block/Sector Unlock command Sequence Diagram (QPI)

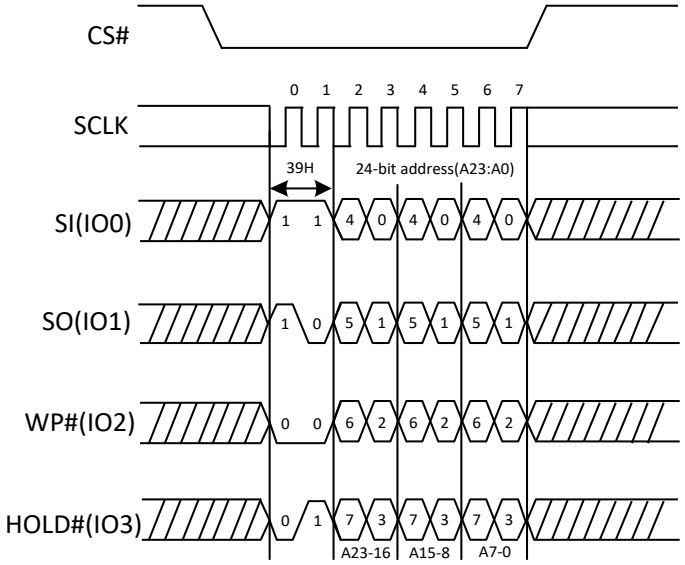


Figure 38d. Read Individual Block/Sector lock command Sequence Diagram

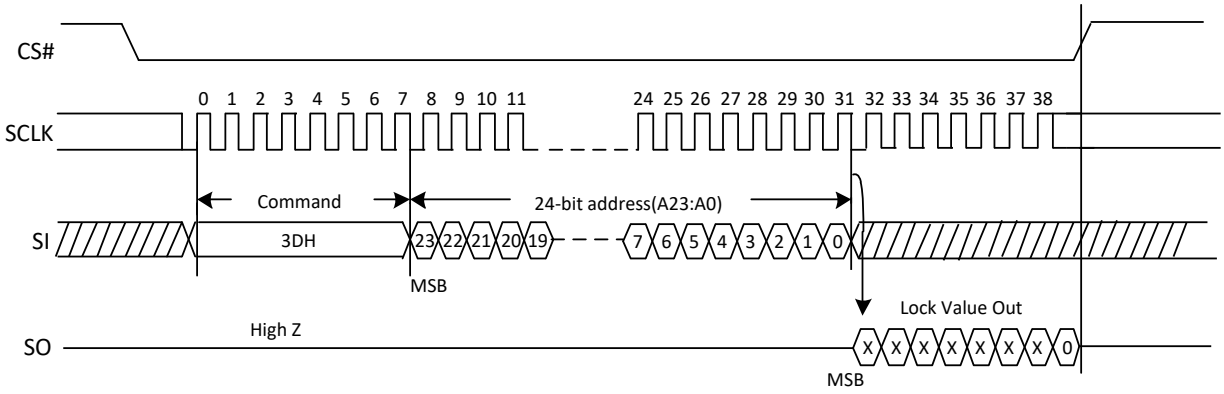
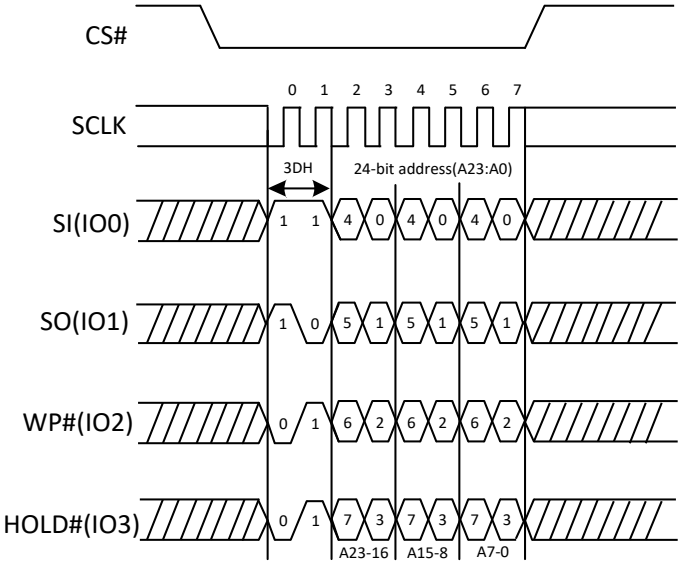
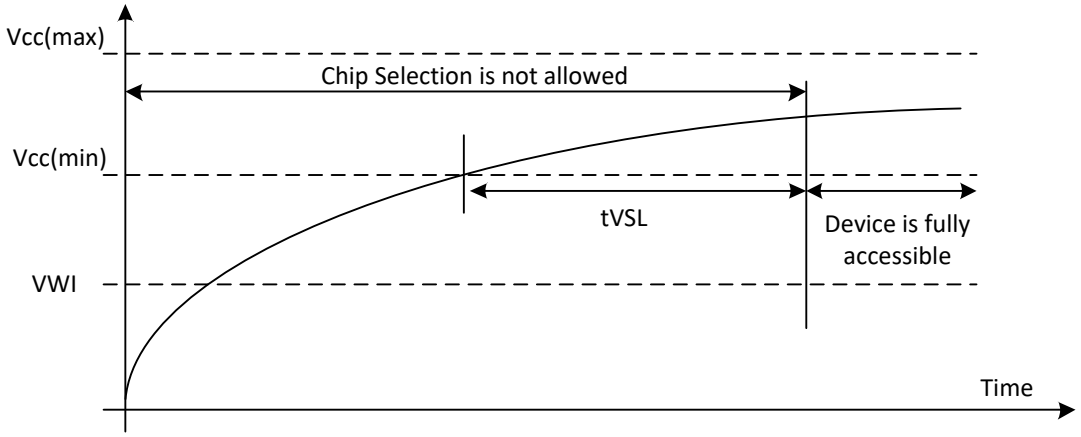


Figure 38e. Read Individual Block/Sector lock command Sequence Diagram (QPI)



6. ELECTRICAL CHARACTERISTICS

6.1. Power-on Timing



Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
t_{VSL}	VCC(min) To CS# Low	200		us
V_{WI}	Write Inhibit Voltage	-	1.5	V

6.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH). All Status Register bits except S22 bits are 0, S22 bit is 1.

6.3. Absolute Maximum Ratings

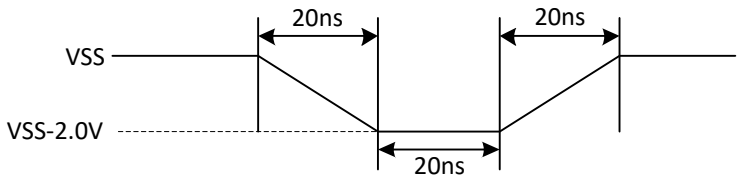
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

6.4. Capacitance Measurement Condition

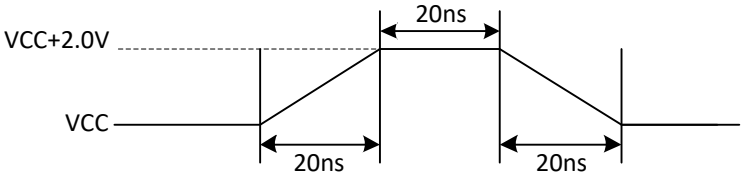
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage		0.5VCC		V	

Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



6.5. DC Characteristics

(T=-40℃~85℃,VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC VIN=VCC or VSS		12	30	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC VIN=VCC or VSS		0.4	8	μA
I_{CC3}	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 133MHz, Q=Open(*1,*2 I/O)		13	16	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*1,*2 I/O)		6	10	mA
		CLK=0.1VCC/0.9VCC at 133MHz, Q=Open(*4 I/O)		16	20	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*4 I/O)		10	16	mA
I_{CC4}	Operating Current(PP)	CS#=VCC			20	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC			20	mA
I_{CC6}	Operating Current(SE, BE, CE)	CS#=VCC			20	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL=1.6mA			0.4	V
V_{OH}	Output High Voltage	IOH=-100uA	VCC-0.2			V

Note:
1. Typical values given for TA=25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

6.6. AC Characteristics

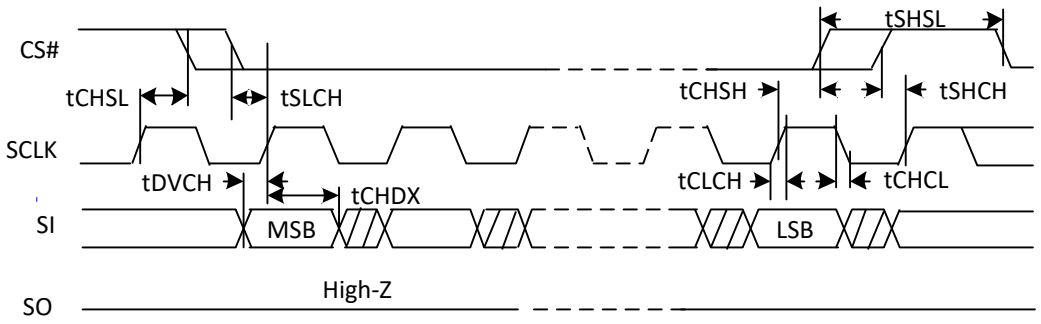
(T=-40℃~85℃,VCC=1.65~2.0V， CL=30pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
fC1	Serial Clock Frequency For: all command except for 03H, EBH, BBH, EDH under SPI mode	D.C.		133	MHz
fC2	Serial Clock Frequency For: EBH, BBH and QPI instructions	D.C.		108	MHz
fC3	Clock frequency DTR instructions EDH	D.C.		96	MHz
fR	Serial Clock Frequency For: Read (03H)	D.C.		80	MHz
tCLH(1)	Serial Clock High Time	45%PC			ns
tCLL(1)	Serial Clock Low Time	45%PC			ns
tCLCH	Serial Clock Rise Time(Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time(Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL	CS# High Time (read/write)	20			ns
tSHQZ	Output Disable Time			8	ns
tCLQV	Clock Low To Output Valid			5	ns
tCLQX	Output Hold Time	1			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	Hold# Low Setup Time(relative to Clock)	5			ns
tHHCH	Hold# High Setup Time(relative to Clock)	5			ns
tCHHL	Hold# High Hold Time(relative to Clock)	5			ns
tCHHH	Hold# Low Hold Time(relative to Clock)	5			ns
tHLQZ	Hold# Low To High-Z Output			6	ns
tHHQX	Hold# High To Low-Z Output			6	ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tDP	CS# High To Deep Power-Down Mode			3	us
tRES1	CS# High To Standby Mode Without Electronic Signature Read			6	us
tRES2	CS# High To Standby Mode With Electronic Signature Read			3	us
tRST	CS# High To Next Command After Reset			20	us
tSUS	CS# High To Next Command After Suspend			20	us
tRS	Latency Between Resume And Next Suspend	100			us
tW	Write Status Register Cycle Time		1	20	ms
tPP	Page Programming Time		0.4	1	ms
tSE	Sector Erase Time		40	300	ms
tBE1	Block Erase Time (32K Bytes)		0.12	1	s

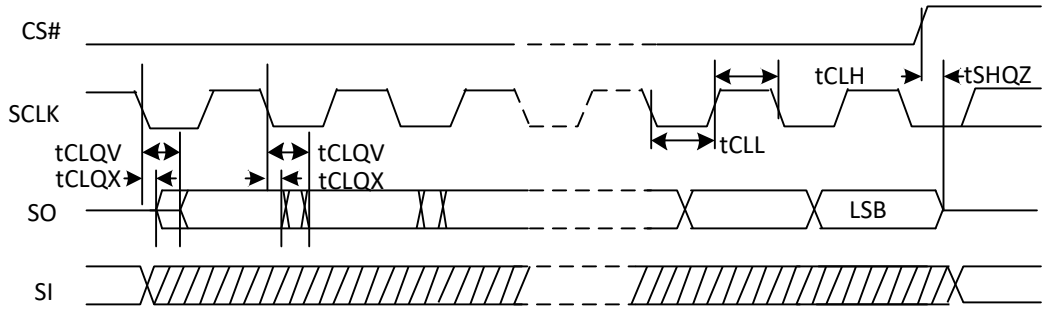
tBE2	Block Erase Time (64K Bytes)		0.15	1.2	s
tCE	Chip Erase Time		20	50	s

Note:
1. Clock high or Clock low must be more than or equal to 45%PC. PC=1/fC(MAX).
2. Typical values given for TA=25°C. Value guaranteed by design and/or characterization, not 100% tested in production.

Serial Input Timing

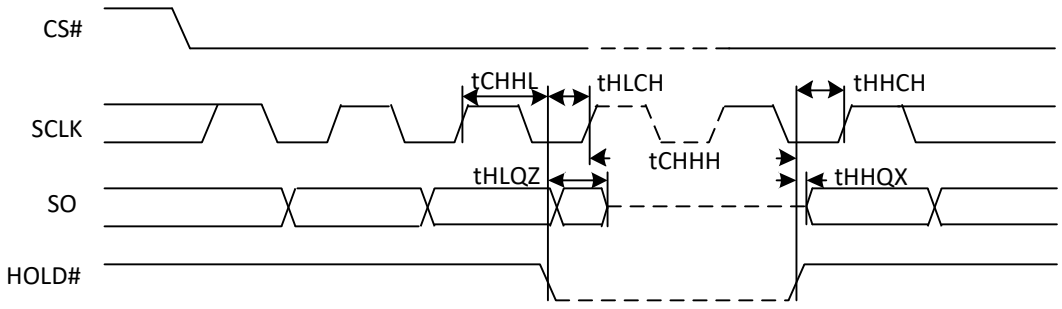


Output Timing



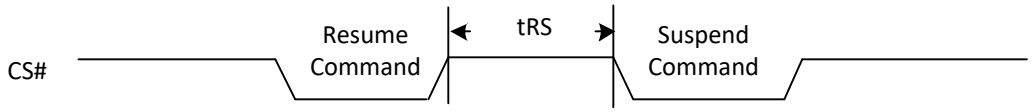
Least significant address bit (LSB) in

Hold Timing



SI do not care during HOLD operation

Resume to Suspend Timing Diagram



7. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following

XT 25Q 64D SS I G U

Company Prefix

XT = XTX

Product Family

25Q = 1.65~2.0V Serial Flash Memory
with 4KB Uniform-Sector

Product Density

64D = 64M bit

Product Package

SS = 8-pin SOP8 (208mil)
WO = WSON8 6x5
WL = WLCSP-WL
LC = WLCSP-LC

Temperature & Moisture Sensitivity Level

I = Industrial Level Temp. (-40℃ to +85℃), MSL3

Green Code

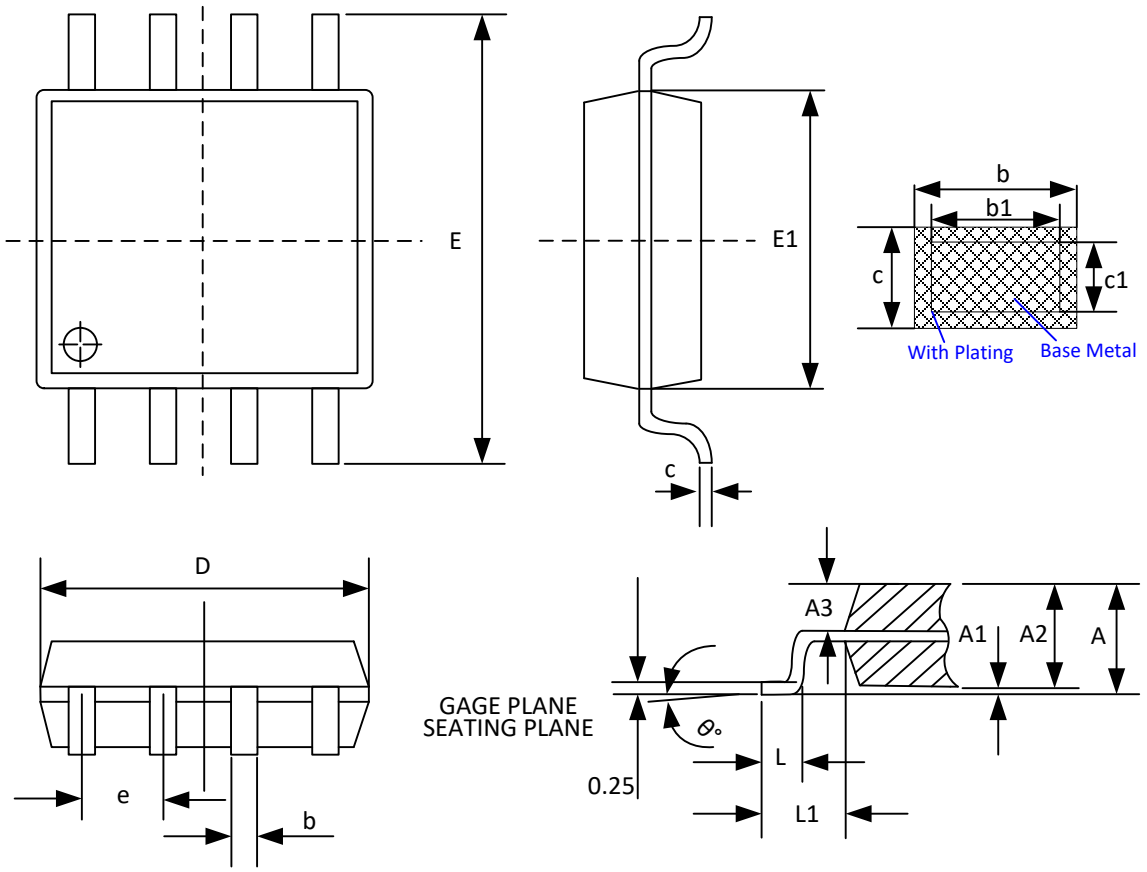
G = Green/Reach Package

Product Carrier

U = Tube; **T** = Tape & Reel; **A** = Tray

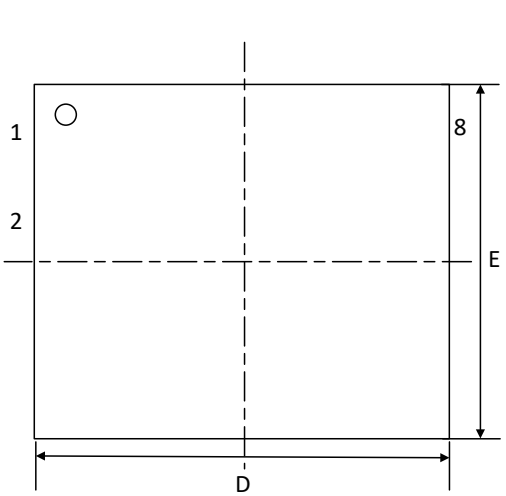
8. PACKAGE INFORMATION

8.1. Package SOP8 208mil

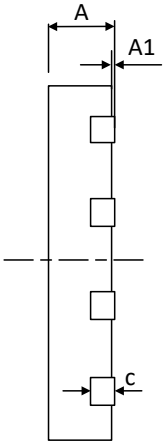


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.75	1.95	2.15
A1	0.05	0.15	0.25
A2	1.70	1.80	1.90
A3	0.75	0.80	0.85
b	0.33	—	0.51
b1	0.30	—	0.48
c	0.17	—	0.25
c1	0.15	0.20	0.23
D	5.13	5.23	5.33
E	7.70	7.90	8.10
E1	5.18	5.28	5.38
e	1.27 BSC		
L	0.50	0.65	0.80
L1	1.31 REF		
θ	0°	—	8°

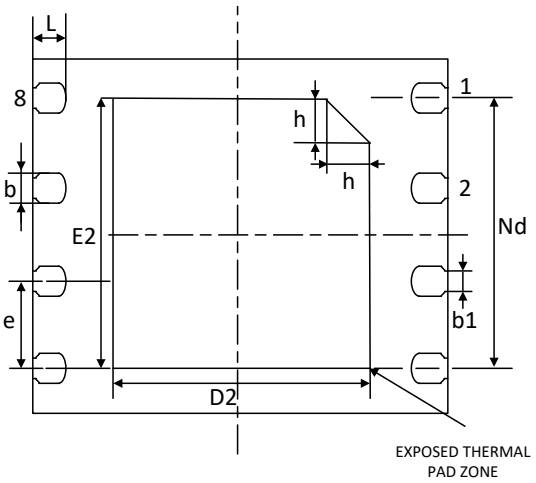
8.2. Package WSON8 6x5mm



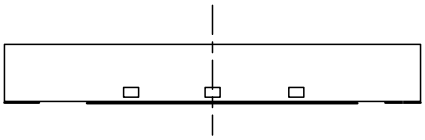
TOP VIEW



SIDE VIEW



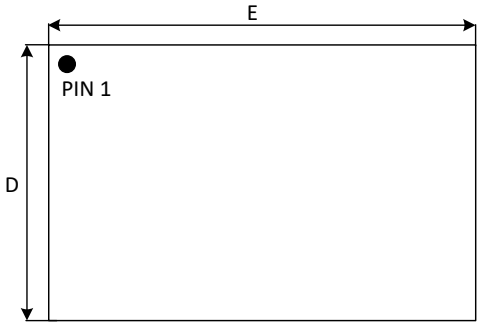
BOTTOM VIEW



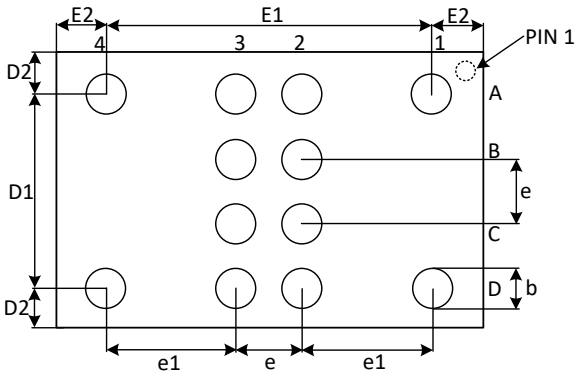
SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
b1		0.25 REF	
c	0.18	0.20	0.25
D	5.90	6.00	6.10
Nd		3.81 BSC	
e		1.27 BSC	
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.90	4.00	4.10
L	0.55	0.60	0.65
h	0.30	0.35	0.40

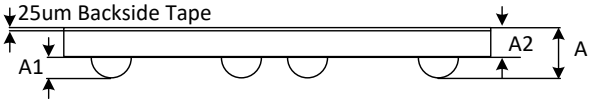
8.3. Package WLCSP-WL



TOP VIEW



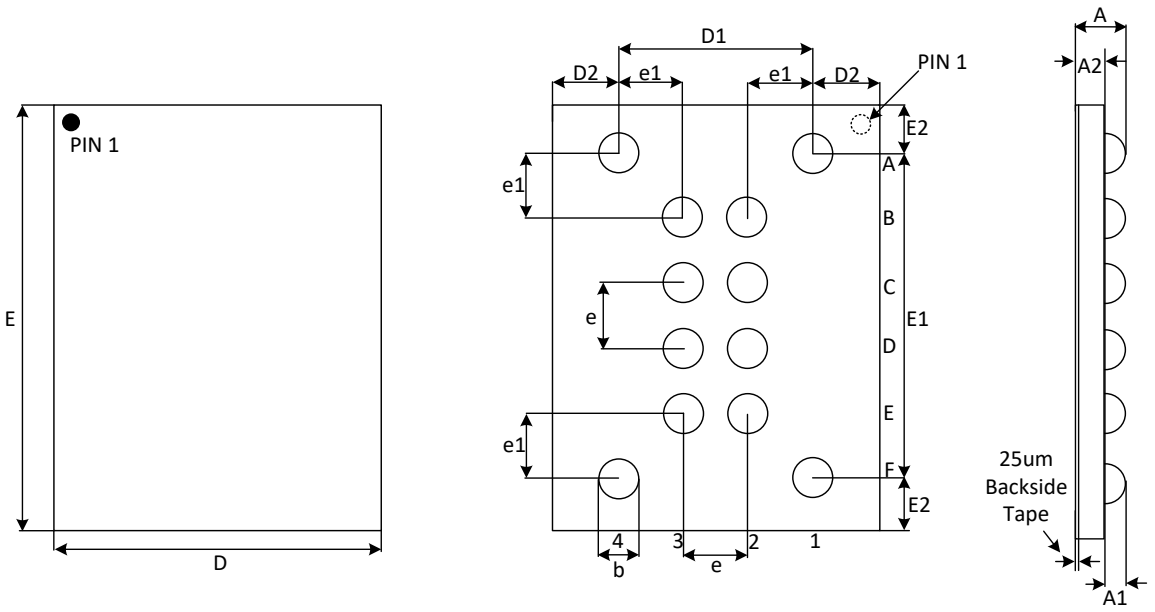
BOTTOM VIEW



SIDE VIEW

Symbol / Unit		A	A1	A2	D1	E1	e	e1	b
mm	Min	0.430	0.140	0.290	1.500 BSC	2.100 BSC	0.500 BSC	0.800 BSC	0.270
	Typ	0.480	0.165	0.315					0.300
	Max	0.530	0.190	0.340					0.330

8.4. Package WLCSP-LC



TOP VIEW **BOTTOM VIEW** **SIDE VIEW**

Symbol / Unit		A	A1	A2	D1	E1	e	e1	b
mm	Min	0.430	0.140	0.290	1.300 BSC	2.300 BSC	0.500 BSC	0.400 BSC	0.270
	Typ	0.480	0.165	0.315					0.300
	Max	0.530	0.190	0.340					0.330

9. REVISION HISTORY

Revision	Description	Date
1.0	Initial version	Dec-8-2020
1.1	Added CE operation current -> 20mA max Revise unit for tRST Deleted Latch up Characteristics, refer to Qualification Report. Adjust command C0H's description to add P2 Updated SFDP table Operating Voltage range 1.65~2.1V -> 1.65~2.0V	Mar-23-2021
1.2	Update POD of SOP8 208mil, WSON8 6x5mm and WLCSP-LC	Mar-29-2021
1.3	Correct pin name on WLCSP-LC connection diagram Changed 3EH in SFDP Table and update SFDP Table	Apr-23-2021