



Technology Limited

NOR MCP Specification

64M bit SPI NOR Flash

+

64M bit QPI pSRAM

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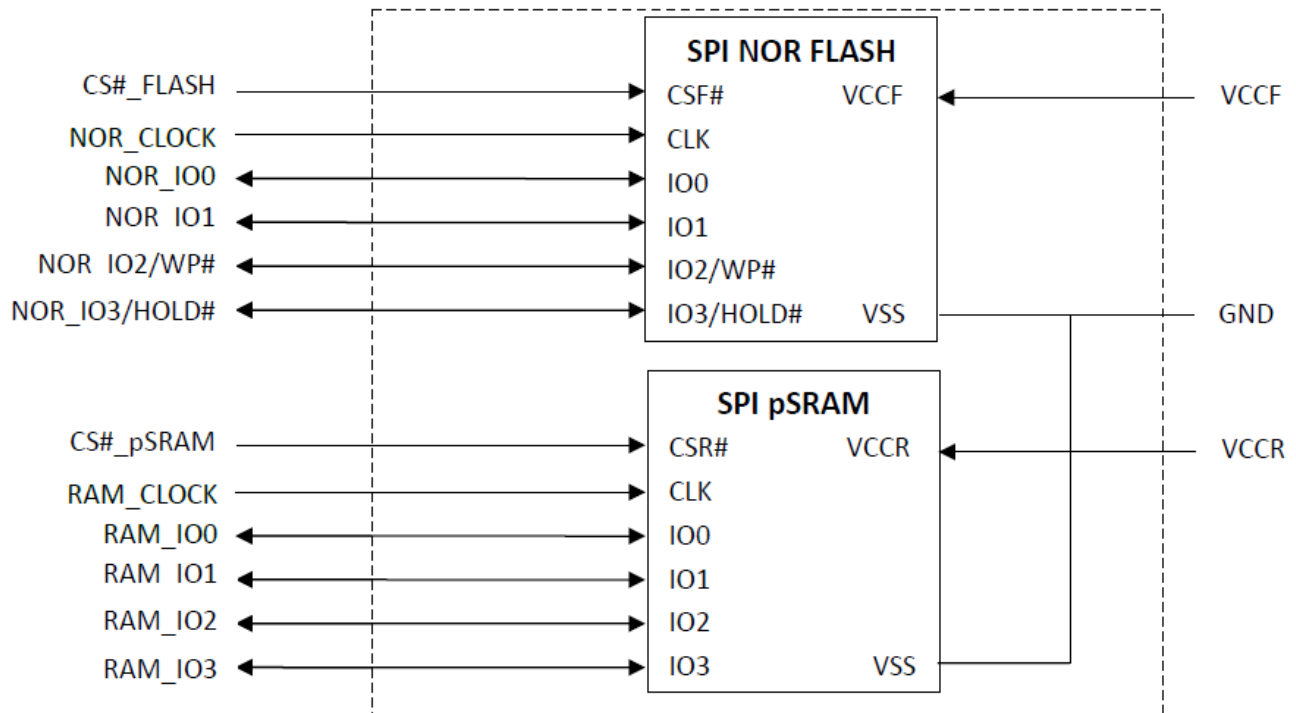
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Introduction

XTX NOR MCP is an integration of a high performance SPI NOR Flash plus a high-speed QPI pSRAM, it can be used for storing user data and/or executable code, audio and video file cache.

The package size is only 6x5mm and suitable for wearable device design application.

NOR MCP Block Diagram



SPI NOR Features

- **64M -bit Serial Flash**
 - 8192K-byte
 - 256 bytes per programmable page
- **Support SFDP & Unique ID**
- **Standard, Dual, Quad SPI**
 - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
 - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
 - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
 - QPI: SCLK, CS#, IO0, IO1, IO2, IO3
- **Flexible Architecture**
 - Sector of 4K-byte
 - Block of 32/64k-byte
- **Advanced security Features**
 - 4*256-Byte Security Registers With OTP Lock
- **Software/Hardware Write Protection**
 - Write protect all/portion of memory via software
 - Enable/Disable protection with WP# Pin
 - Top or Bottom, Sector or Block selection
- **Package Options**
 - See 1.1 Available Ordering OPN
 - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- **Temperature Range & Moisture Sensitivity Level**
 - Industrial Level Temperature. (-40°C to +85°C), MSL3
- **Low Power Consumption**
 - 12mA typical standby current
 - 0.1uA typical power down current
- **Single Power Supply Voltage: Full voltage range:**
 - 2.7~3.6V
- **Minimum 100,000 Program/Erase Cycle**
- **High Speed Clock Frequency**
 - 108MHz for fast read with 30PF load
 - Dual I/O Data transfer up to 216Mbits/s
 - Quad I/O Data transfer up to 344Mbits/s
 - QPI Mode Data transfer up to 288Mbits/s
 - Continuous Read With 8/16/32/64-byte Wrap
- **Program/Erase Speed**
 - Page Program time: 300us typical
 - Sector Erase time: 60ms typical
 - Block Erase time: 0.15/0.25s typical
 - Chip Erase time: 22s typical

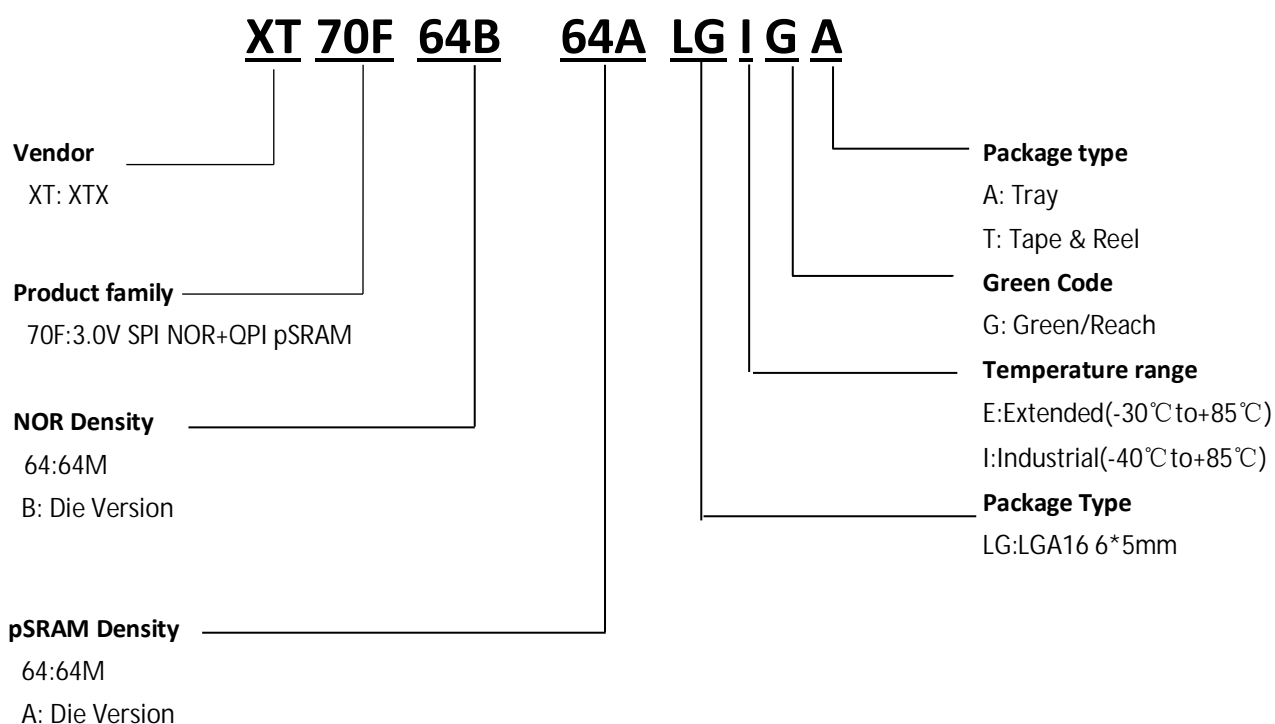
pSRAM Features

- Single Supply Voltage:
 - VDD=2.7 to 3.6V
- Interface: SPI/QPI with SDR mode
- Performance: Clock rate up to
 - 109MHz (Wrap Mode)PKG*
 - 84MHz (Linear Burst Mode)
- Organization: 64Mb, 8M x 8bits
- Addressable bit range: A[22:0]
- Page Size: 1024 bytes
- Refresh: Self-managed
- Maximum Standby Current:
 - 350 μ A @ 105°C
 - 250 μ A @ 85°C
 - 140 μ A @ 25°C
- 50 Ω Output Drive Strength LVCMOS.
- Linear Burst (continuous) or 32 byte wrapped burst via toggle command.
- Linear Burst is supported up to 84MHz and can cross page boundary as long as tCEM is met.
- 1K byte or 32 byte wrapped burst via toggle command as long as tCEM is met.
- Software reset.

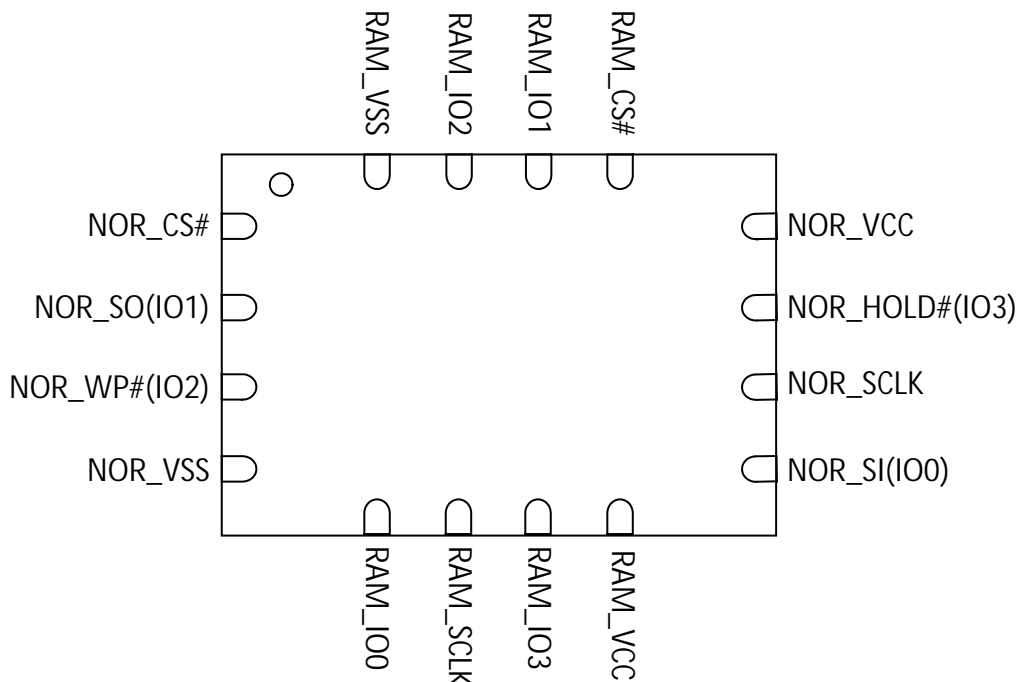
Ordering information

| OPN | NOR FLASH | pSRAM | Package Type | Package Carrier |
|------------------|-----------|---------|--------------|-----------------|
| XT70F64B64ALGIGT | 64M bit | 64M bit | LGA16 5*6mm | Tape & Reel |
| XT70F64B64ALGIGA | 64M bit | 64M bit | LGA16 5*6mm | Tray |

Part number description



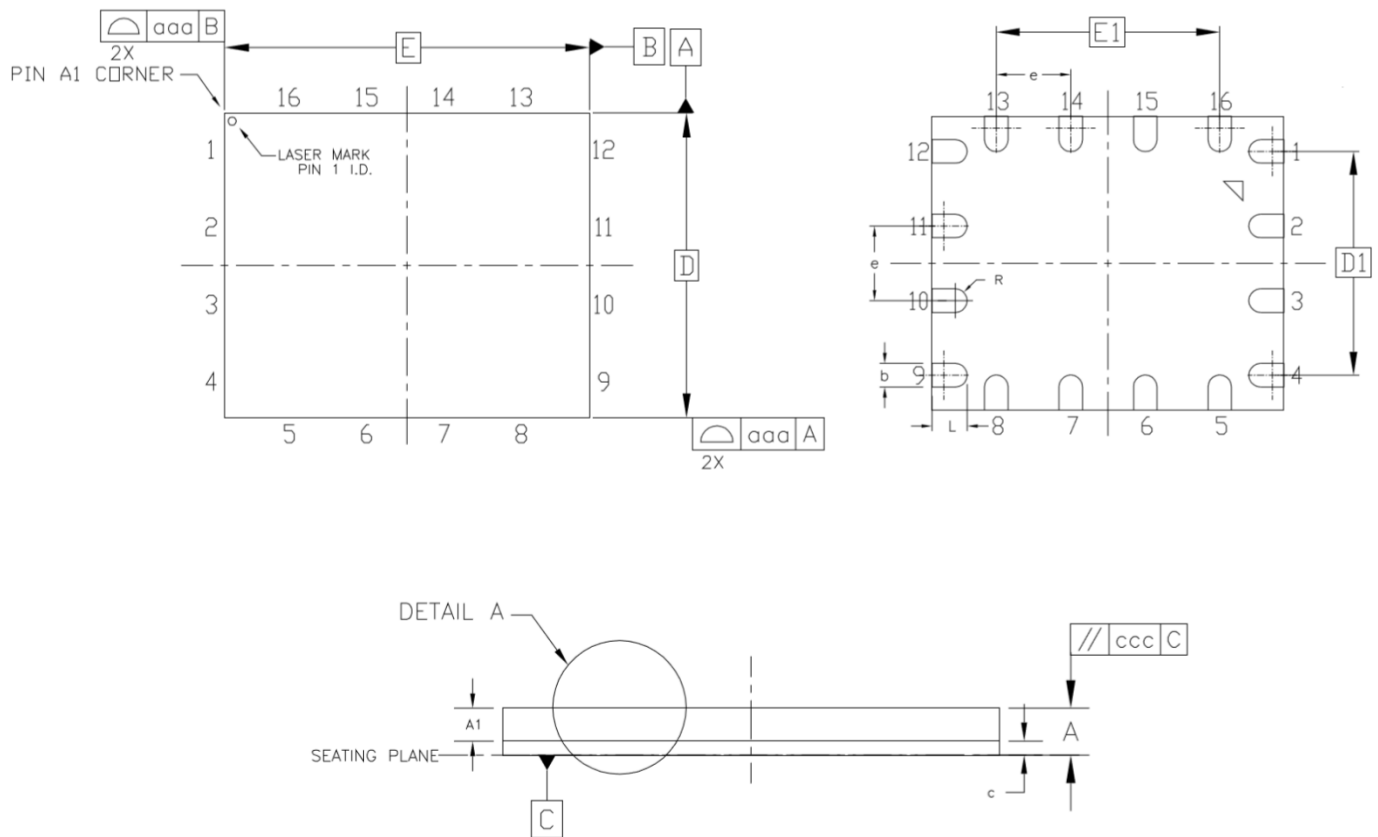
Pin Assignments



Pin Description

| Pin Name | I/O | Description |
|-----------------|--------|--|
| NOR_CS# | Input | Chip Select Input |
| NOR_SO(IO1) | IO | Data Output (DataInputOutput1) |
| NOR_WP#(IO2) | IO | Write Protect Input (DataInputOutput2) |
| NOR_VSS | | Ground |
| NOR_SI(IO0) | IO | Data Input (DataInputOutput0) |
| NOR_SCLK | Input | Serial Clock Input |
| NOR_HOLD# (IO3) | IO | Hold or Reset Input (DataInputOutput3) |
| NOR_VCC | | Power Supply |
| RAM_VCC | Power | Core supply 3.3V |
| RAM_VSS | Ground | Core supply ground |
| RAM_CS# | Input | Chip select, active low. When CE#=1, chip is in standby state |
| RAM_SCLK | Input | Clock Signal |
| RAM_IO0 | IO | Serial Input under SPI Mode Function, IO[0] under QPI Mode Function |
| RAM_IO1 | IO | Serial Output under SPI Mode Function, IO[1] under QPI Mode Function |
| RAM_IO2 | IO | IO[2] under QPI Mode Function |
| RAM_IO3 | IO | IO[3] under QPI Mode Function |

Package Dimension



| Symbol | Dimensions in Millimeters | | |
|--------|---------------------------|------|------|
| | Min | Norm | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.53 BASIC | | |
| c | 0.18 | 0.22 | 0.26 |
| D | 4.90 | 5.00 | 5.10 |
| D1 | 3.81 BASIC | | |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 3.81 BASIC | | |
| e | 1.27 BASIC | | |
| b | 0.35 | 0.40 | 0.45 |
| L | 0.55 | 0.60 | 0.65 |
| R | 0.20 REF | | |
| aaa | 0.10 | | |
| ccc | 0.20 | | |

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64M bit SPI NOR

1.1. GENERAL DESCRIPTION

The XT25F64B (64M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). The Dual I/O data is transferred with speed of 216Mbits/s and the Quad I/O & Quad output data is transferred with speed of 344Mbits/s.

1.2. MEMORY ORGANIZATION

| Each Device has | Each block has | Each sector has | Each page has | Remark |
|-----------------|----------------|-----------------|---------------|---------|
| 8M | 64K/32K | 4K | 256 | bytes |
| 32K | 256/128 | 16 | - | pages |
| 2K | 16/8 | - | - | sectors |
| 128/256 | - | - | - | blocks |

UNIFORM BLOCK SECTOR ARCHITECTURE

64K Bytes Block Sector Architecture

| Block | Sector | Address range | |
|-------|--------|---------------|-----------|
| 127 | 2047 | 7FF000H | 7FFFFFFH |
| | | | |
| | 2032 | 7F0000H | 7FOFFFFH |
| 126 | 2031 | 7EF000H | 7EFFFFFFH |
| | | | |
| | 2016 | 7E0000H | 7EOFFFFH |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| 2 | 47 | 02F000H | 02FFFFFFH |
| | | | |
| | 32 | 020000H | 020FFFFH |
| 1 | 31 | 01F000H | 01FFFFFFH |
| | | | |
| | 16 | 010000H | 010FFFFH |
| 0 | 15 | 00F000H | 00FFFFFFH |
| | | | |
| | 0 | 000000H | 000FFFFH |

1.3. DEVICE OPERATION

SPI Mode

Standard SPI

The device features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Note: "WP#" & "HOLD#" pin require external pull-up.

Dual SPI

The device supports Dual SPI operation when using the "Dual Output Fast Read" and "Dual I/O Fast Read" (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Note: "WP#" & "HOLD#" pin require external pull-up.

Quad SPI

The device supports Quad SPI operation when using the "Quad Output Fast Read", "Quad I/O Fast Read", "Quad I/O Word Fast Read" (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

QPI

The device supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the "Enable the QPI (38H)" command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. "Enable the QPI (38H)" and "Disable the QPI (FFH)" commands are used to switch between these two modes. Upon power-up and after software reset using "Reset (99H)" command, the default state of the device is Standard/Dual/Quad SPI mode. The QPI mode requires the non-volatile Quad Enable bit (QE) in Status Register to be set.

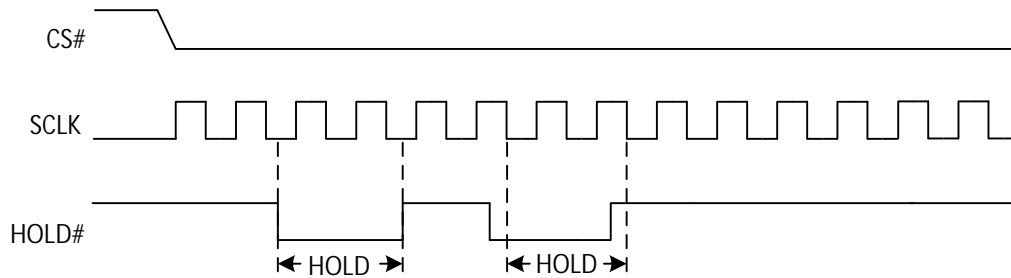
Hold

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

Both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure1.Hold Condition



1.4. DATA PROTECTION

The 64M provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
 - Power-Up
 - Write Disable (WRDI)
 - Write Status Register (WRSR)
 - Page Program (PP)
 - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
- Hardware Protection Mode: WP# going low to protected the BP0~BP4 bits and SRP bit.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

Table1.0 64M Protected area size (CMP=0)

| Status Register Content | | | | | Memory Content | | | |
|-------------------------|-----|-----|-----|-----|----------------|------------------|---------|--------------|
| BP4 | BP3 | BP2 | BP1 | BP0 | Blocks | Addresses | Density | Portion |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 126 to 127 | 7E0000H-7FFFFFFH | 128KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 124 to 127 | 7C0000H-7FFFFFFH | 256KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 120 to 127 | 780000H-7FFFFFFH | 512KB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 112 to 127 | 700000H-7FFFFFFH | 1MB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 96 to 127 | 600000H-7FFFFFFH | 2MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 64 to 127 | 400000H-7FFFFFFH | 4MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 to 1 | 000000H-01FFFFH | 128KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 to 3 | 000000H-03FFFFH | 256KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 to 7 | 000000H-07FFFFH | 512KB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 to 15 | 000000H-0FFFFFFH | 1MB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 to 31 | 000000H-1FFFFFFH | 2MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 to 63 | 000000H-3FFFFFFH | 4MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 to 127 | 000000H-7FFFFFFH | 8MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 127 | 7FF000H-7FFFFFFH | 4KB | Top Block |
| 1 | 0 | 0 | 1 | 0 | 127 | 7FE000H-7FFFFFFH | 8KB | Top Block |
| 1 | 0 | 0 | 1 | 1 | 127 | 7FC000H-7FFFFFFH | 16KB | Top Block |
| 1 | 0 | 1 | 0 | X | 127 | 7F8000H-7FFFFFFH | 32KB | Top Block |
| 1 | 0 | 1 | 1 | 0 | 127 | 7F8000H-7FFFFFFH | 32KB | Top Block |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000H-000FFFH | 4KB | Bottom Block |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000H-001FFFH | 8KB | Bottom Block |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000H-003FFFH | 16KB | Bottom Block |
| 1 | 1 | 1 | 0 | X | 0 | 000000H-007FFFH | 32KB | Bottom Block |
| 1 | 1 | 1 | 1 | 0 | 0 | 000000H-007FFFH | 32KB | Bottom Block |

Table1.1 64M Protected area size (CMP=1)

| Status Register Content | | | | | Memory Content | | | |
|-------------------------|-----|-----|-----|-----|----------------|------------------|---------|-------------|
| BP4 | BP3 | BP2 | BP1 | BP0 | Blocks | Addresses | Density | Portion |
| X | X | 0 | 0 | 0 | ALL | 000000H-7FFFFFFH | ALL | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 to 125 | 000000H-7DFFFFH | 8064KB | Lower 63/64 |
| 0 | 0 | 0 | 1 | 0 | 0 to 123 | 000000H-7BFFFFH | 7936KB | Lower 31/32 |
| 0 | 0 | 0 | 1 | 1 | 0 to 119 | 000000H-77FFFFH | 7680KB | Lower 15/16 |
| 0 | 0 | 1 | 0 | 0 | 0 to 111 | 000000H-6FFFFFFH | 7MB | Lower 7/8 |
| 0 | 0 | 1 | 0 | 1 | 0 to 95 | 000000H-5FFFFFFH | 6MB | Lower 3/4 |
| 0 | 0 | 1 | 1 | 0 | 0 to 63 | 000000H-3FFFFFFH | 4MB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 2 to 127 | 020000H-7FFFFFFH | 8064KB | Upper 63/64 |
| 0 | 1 | 0 | 1 | 0 | 4 to 127 | 040000H-7FFFFFFH | 7936KB | Upper 31/32 |
| 0 | 1 | 0 | 1 | 1 | 8 to 127 | 080000H-7FFFFFFH | 7680KB | Upper 15/16 |
| 0 | 1 | 1 | 0 | 0 | 16 to 127 | 100000H-7FFFFFFH | 7MB | Upper 7/8 |
| 0 | 1 | 1 | 0 | 1 | 32 to 127 | 200000H-7FFFFFFH | 6MB | Upper 3/4 |
| 0 | 1 | 1 | 1 | 0 | 64 to 127 | 400000H-7FFFFFFH | 4MB | Upper 1/2 |
| X | X | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 to 127 | 000000H-7FEFFFFH | 8188KB | L-2047/2048 |
| 1 | 0 | 0 | 1 | 0 | 0 to 127 | 000000H-7FDFFFFH | 8184KB | L-1023/1024 |
| 1 | 0 | 0 | 1 | 1 | 0 to 127 | 000000H-7FBFFFFH | 8176KB | L-511/512 |
| 1 | 0 | 1 | 0 | X | 0 to 127 | 000000H-7F7FFFFH | 8160KB | L-255/256 |
| 1 | 0 | 1 | 1 | 0 | 0 to 127 | 000000H-7F7FFFFH | 8160KB | L-255/256 |
| 1 | 1 | 0 | 0 | 1 | 0 to 127 | 001000H-7FFFFFFH | 8188KB | U-2047/2048 |
| 1 | 1 | 0 | 1 | 0 | 0 to 127 | 002000H-7FFFFFFH | 8184KB | U-1023/1024 |
| 1 | 1 | 0 | 1 | 1 | 0 to 127 | 004000H-7FFFFFFH | 8176KB | U-511/512 |
| 1 | 1 | 1 | 0 | X | 0 to 127 | 008000H-7FFFFFFH | 8160KB | U-255/256 |
| 1 | 1 | 1 | 1 | 0 | 0 to 127 | 008000H-7FFFFFFH | 8160KB | U-255/256 |

1.5. STATUS REGISTER

| S15 | S14 | S13 | S12 | S11 | S10 | S9 | S8 |
|----------|-----|----------|-----|-----|-----|----|------|
| Reserved | CMP | HOLD/RST | WPS | LB1 | LB0 | QE | SRP1 |

| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |
|------|-----|-----|-----|-----|-----|-----|-----|
| SRP0 | BP4 | BP3 | BP2 | BP1 | BP0 | WEL | WIP |

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, BP0) bits are 1 and CMP=1.

SRP1, SRP0 bits.

The Status Register Protect (SRP) bit is non-volatile Read/Write bits in the status register. The SRP bit controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

| SRP1 | SRP0 | WP# | Status Register | Description |
|------|------|-----|------------------------------|--|
| 0 | 0 | X | Software Protected | The Status Register can be written to after a Write Enable command, WEL=1.(Default) |
| 0 | 1 | 0 | Hardware Protected | WP#=0, the Status Register locked and can not be written until the next power-up. |
| 0 | 1 | 1 | Hardware Unprotected | WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1. |
| 1 | 0 | X | Power Supply Lock-Down(1)(2) | Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle. |
| 1 | 1 | X | One-Time Program(2) | Status Register is permanently protected and cannot be written to. |

NOTE:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact XTX for details.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground).

LB bit.

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register (S10) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 using the Write Register instruction. LB is One Time Programmable, once it's set to 1, the Security Registers will become read-only permanently.

CMP bit.

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

1.6. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table2. Commands

| Command Name | Byte1 | Byte2 | Byte3 | Byte4 | Byte5 | Byte6 | n-Bytes |
|---|--------|--------------------|-------------------|------------|------------|-------------|--------------|
| Write Enable | 06H | | | | | | |
| Write Enable for Volatile Status Register | 50H | | | | | | |
| Write Disable | 04H | | | | | | |
| Read Status Register | 05H | (S7-S0) | | | | | (continuous) |
| Read Status Register-1 | 35H | (S15-S8) | | | | | (continuous) |
| Write Status Register | 01H | (S7-S0) | (S15-S8) | | | | (continuous) |
| Read Data | 03H | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | (Next byte) | (continuous) |
| Fast Read | 0BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | (continuous) |
| Dual Output Fast Read | 3BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0)(1) | (continuous) |
| Dual I/O Fast Read | BBH | A23-A8(2) | A7-A0 M7-M0(2) | (D7-D0)(1) | | | (continuous) |
| Quad Output Fast Read | 6BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0)(3) | (continuous) |
| Quad I/O Fast Read | EBH | A23-A0 M7-M0(4) | Dummy(5) | (D7-D0)(3) | | | (continuous) |
| Quad I/O Word Fast Read | E7H | A23-A0 M7-M0(4) | Dummy(6) | (D7-D0)(3) | | | (continuous) |
| Continuous Read Reset | FFH | | | | | | |
| Page Program | 02H | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | (Next byte) | |
| Quad Page Program | 32H | A23-A16 | A15-A8 | A7-A0 | (D7-D0)(3) | | |
| Sector Erase | 20H | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(32KB) | 52H | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(64KB) | D8H | A23-A16 | A15-A8 | A7-A0 | | | |
| Chip Erase | C7/60H | | | | | | |
| Enable QPI | 38H | | | | | | |
| Set Burst with Wrap | 77H | dummy | dummy | dummy | W6-W4 | | |



| | | | | | | | |
|---|-----|----------------|----------------|-------------------|-------------|-------------|--------------|
| Deep Power-Down | B9H | | | | | | |
| Release From Deep | ABH | dummy | dummy | dummy | (DID7-DID0) | | (continuous) |
| Release From Deep Power-Down | ABH | | | | | | |
| Manufacturer/Device ID | 90H | A23-A16 | A15-A8 | A7-A0 | (MID7-MID0) | (DID7-DID0) | (continuous) |
| Manufacturer/Device ID by Dual I/O | 92H | A23-A8 | A7-A0, M[7:0] | (M7-M0) (ID7-ID0) | | | (continuous) |
| Manufacturer/Device ID by Quad I/O | 94H | A23-A0, M[7:0] | dummy | (M7-M0) (ID7-ID0) | | | |
| Read Serial Flash Discoverable Parameters | 5AH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | (continuous) |
| Read Unique ID | 5AH | 00H | 01H | 94H | dummy | (D7-D0) | (continuous) |
| Read Identification | 9FH | (MID7-MID0) | (JDID15-JDID8) | (JDID7-JDID0) | | | (continuous) |
| Erase Security Register(8) | 44H | A23-A16 | A15-A8 | A7-A0 | | | |
| Program Security Register(8) | 42H | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | (Next byte) | |
| Read Security Register(8) | 48H | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | |
| Enable Reset | 66H | | | | | | |
| Reset | 99H | | | | | | |

Table2a. Commands (QPI)

| Command Name | Byte1 | Byte2 | Byte3 | Byte4 | Byte5 | Byte6 |
|--|--------|----------|----------|------------|-----------|-------------|
| Clock Number | (0,1) | (2,3) | (4,5) | (6,7) | (8,9) | (10,11) |
| Write Enable | 06H | | | | | |
| Write Enable for Volatile Status Register | 50H | | | | | |
| Write Disable | 04H | | | | | |
| Read Status Register | 05H | (S7-S0) | | | | |
| Read Status Register-1 | 35H | (S15-S8) | | | | |
| Write Status Register | 01H | (S7-S0) | (S15-S8) | | | |
| Page Program | 02H | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | (Next byte) |
| Sector Erase | 20H | A23-A16 | A15-A8 | A7-A0 | | |
| Block Erase(32KB) | 52H | A23-A16 | A15-A8 | A7-A0 | | |
| Block Erase(64KB) | D8H | A23-A16 | A15-A8 | A7-A0 | | |
| Chip Erase | C7/60H | | | | | |
| Deep Power-Down | B9H | | | | | |
| Set Read Parameters | C0H | P7-P0 | | | | |
| Fast Read | 0BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) |
| Burst Read with Wrap | 0CH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) |
| Quad I/O Fast Read | EBH | A23-A0 | dummy(5) | (D7-D0)(3) | | |
| Release from Deep Power-Down, And Read Device ID(10) | ABH | dummy | dummy | dummy * N | (ID7-ID0) | |
| Manufacturer/Device ID(11) | 90H | dummyx2 | 00H | dummy * N | MID7~MID0 | (ID7-ID0) |
| Read Serial Flash Discoverable Parameters | 5AH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) |
| Read Unique ID | 5AH | 00H | 01H | 94H | dummy | (D7-D0) |
| Disable QPI | FFH | | | | | |
| Enable Reset | 66H | | | | | |
| Reset | 99H | | | | | |

NOTE:

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

IO0 = (D4, D0,)

IO1 = (D5, D1,)

IO2 = (D6, D2,)

IO3 = (D7, D3,)

4. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Quad I/O Fast Read Data

IO0 = (x, x, x, x, D4, D0,...)

IO1 = (x, x, x, x, D5, D1,...)

IO2 = (x, x, x, x, D6, D2,...)

IO3 = (x, x, x, x, D7, D3,...)

6. Quad I/O Word Fast Read Data

IO0 = (x, x, D4, D0,...)

IO1 = (x, x, D5, D1,...)

IO2 = (x, x, D6, D2,...)

IO3 = (x, x, D7, D3,...)

7. Quad I/O Word Fast Read Data: the lowest address bit must be 0.

8. Security Registers Address:

Security Register1: A23-A16=00H, A15-A8=01H, A7-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A8=02H, A7-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A8=03H, A7-A0= Byte Address.

9. QPI Command, Address, Data input/output format:

CLK# 0 1 2 3 4 5 6 7 8 9 10 11

IO0 = C4, C0, A20, A16, A12, A8, A4, A0, D4, D0, D4, D0

IO1 = C5, C1, A21, A17, A13, A9, A5, A1, D5, D1, D5, D1

IO2 = C6, C2, A22, A18, A14, A10, A6, A2, D6, D2, D6, D2

IO3 = C7, C3, A23, A19, A15, A11, A7, A3, D7, D3, D7, D3

10. QPI mode: Release from Deep Power-Down, And Read Device ID (ABH)

N dummy cycles should be inserted before ID read cycle, refer to C0H command

11. QPI mode: Manufacturer/Device ID (90H)

N dummy cycles should be inserted before ID read cycle, refer to C0H command

Table of ID Definitions:

| Operation Code | MID7-MID0 | ID15-ID8 | ID7-ID0 |
|----------------|-----------|----------|---------|
| 9FH | 0B | 40 | 17 |
| 90H | 0B | | 16 |
| ABH | | | 16 |

1.6.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure2. Write Enable Sequence Diagram

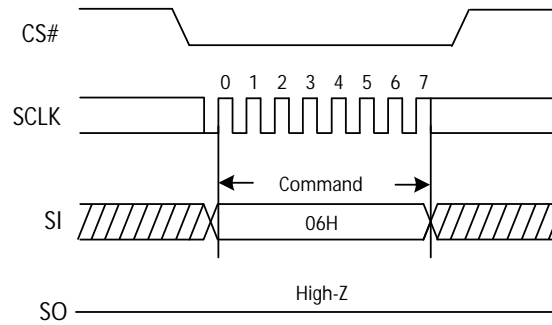
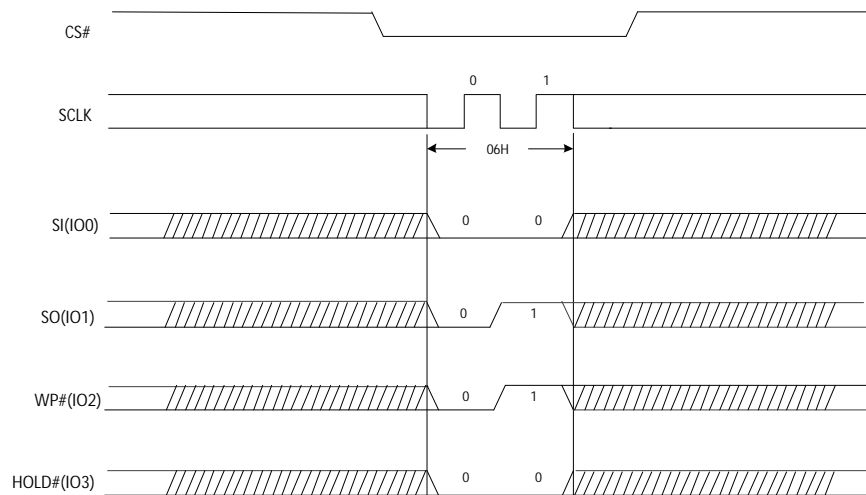
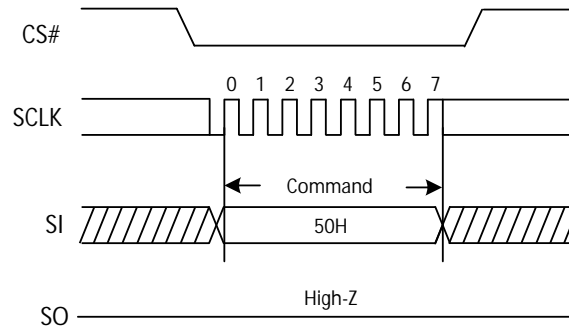
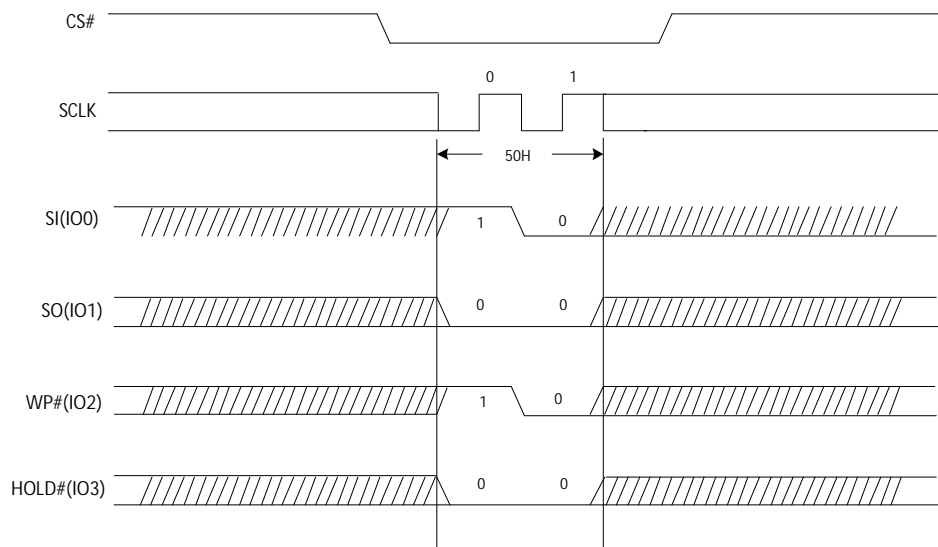


Figure 2a. Write Enable Sequence Diagram (QPI)



1.6.2 Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure3. Write Enable for Volatile Status Register Sequence Diagram

Figure3a. Write Enable for Volatile Status Register Sequence Diagram (QPI)


1.6.3 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low → sending the Write Disable command → CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

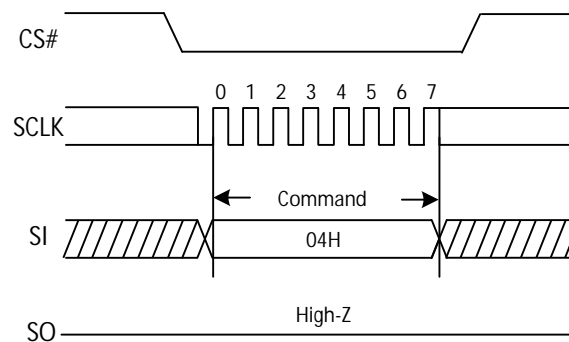
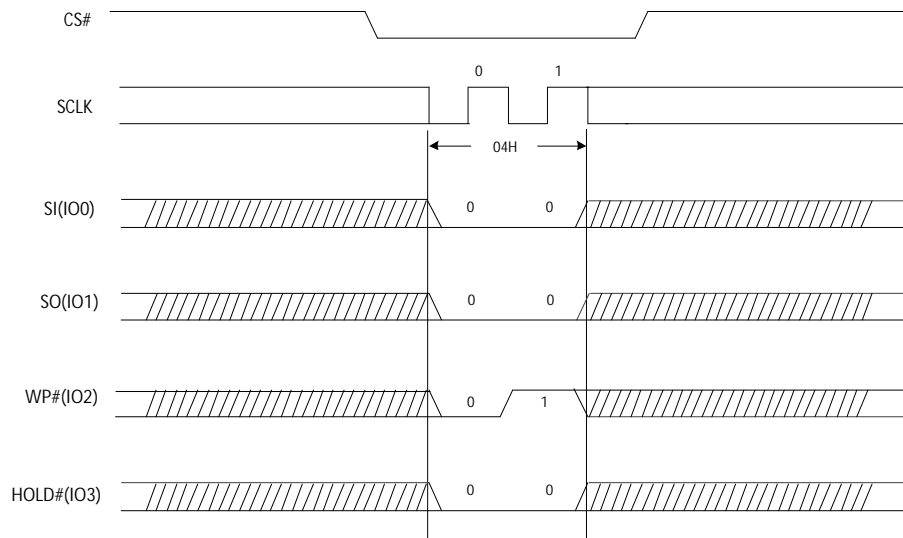
Figure 4. Write Disable Sequence Diagram


Figure 4a. Write Disable Sequence Diagram (QPI)

1.6.4 Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code "05H", the SO will output Status Register bits S7~S0. The command code "35H", the SO will output Status Register bits S15~S8.

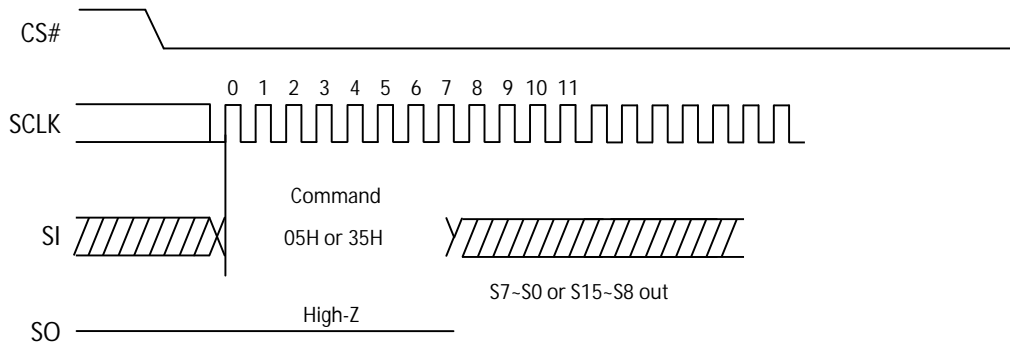
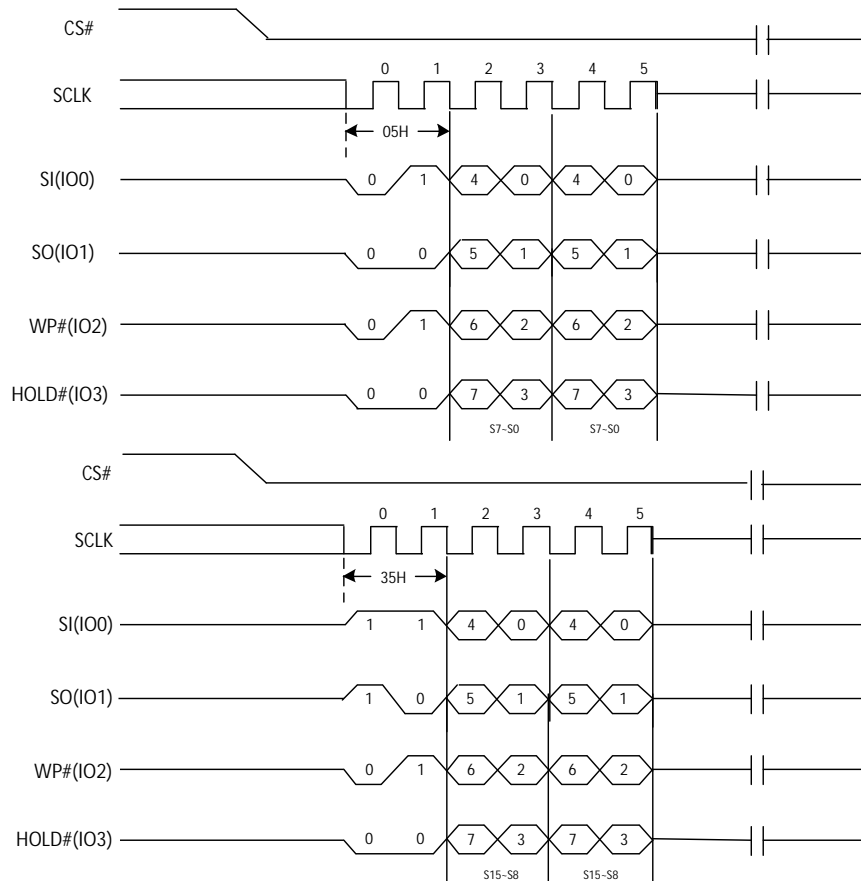
Figure 5. Read Status Register Sequence Diagram

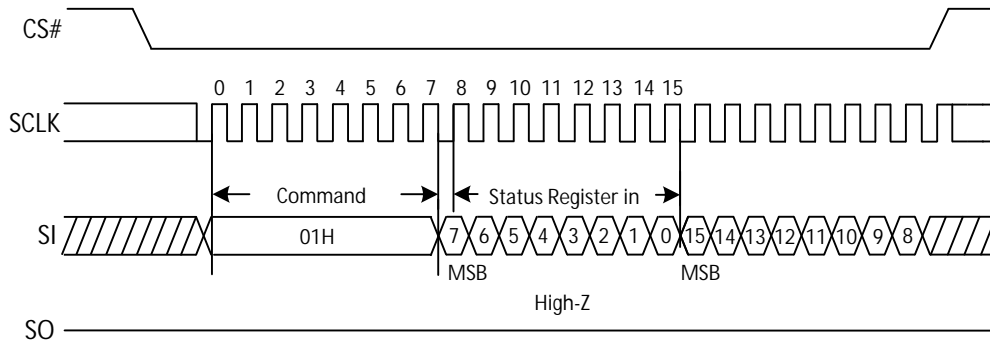
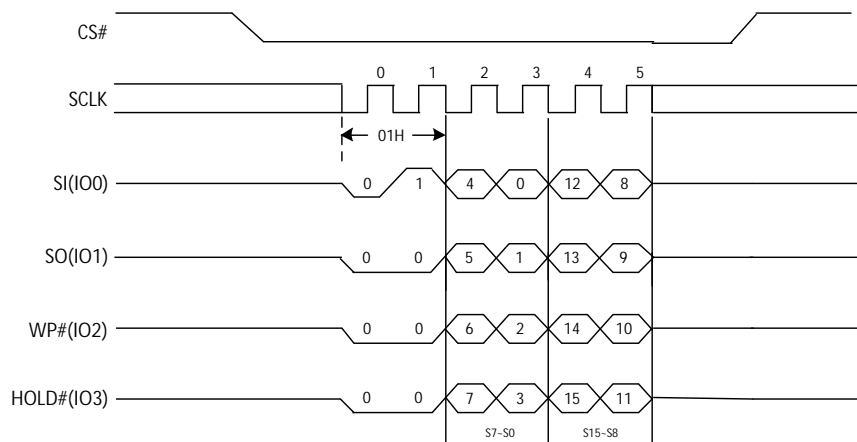
Figure5a. Read Status Register Sequence Diagram (QPI)


1.6.5 Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

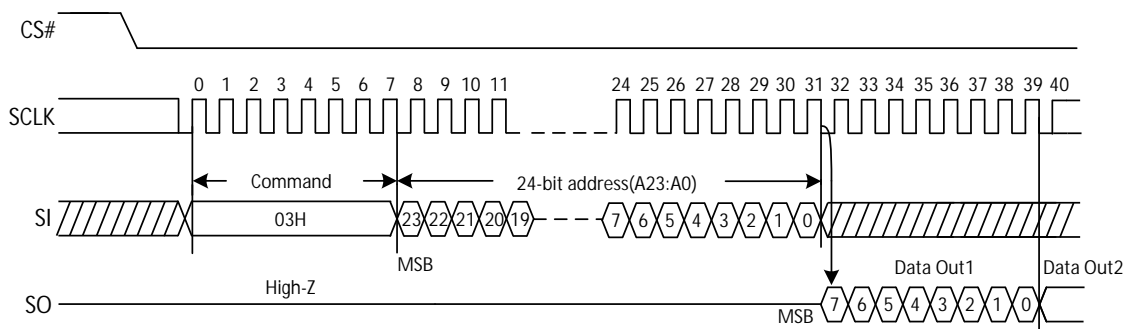
The Write Status Register (WRSR) command has no effect on S15, S13, S12, S11, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the CMP and QE bit will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register can still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

Figure 6. Write Status Register Sequence Diagram

Figure 6a. Write Status Register Sequence Diagram (QPI)


1.6.6 Read Data Bytes (READ) (03H)

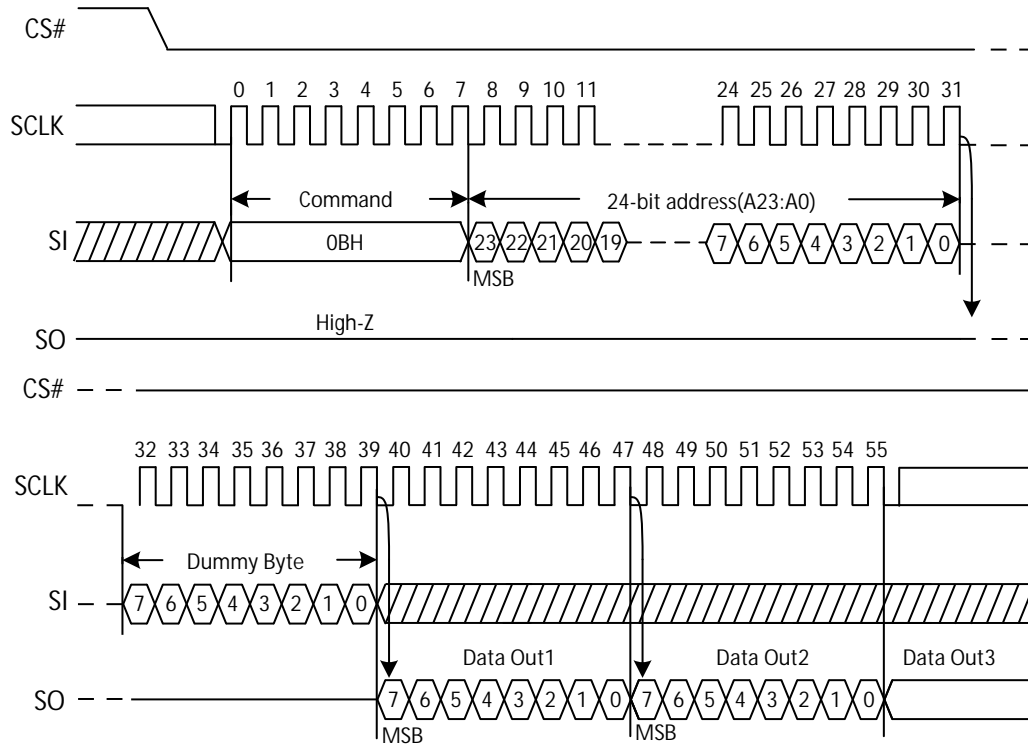
The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_R , during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 7. Read Data Bytes Sequence Diagram


1.6.7 Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for fast reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C , during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

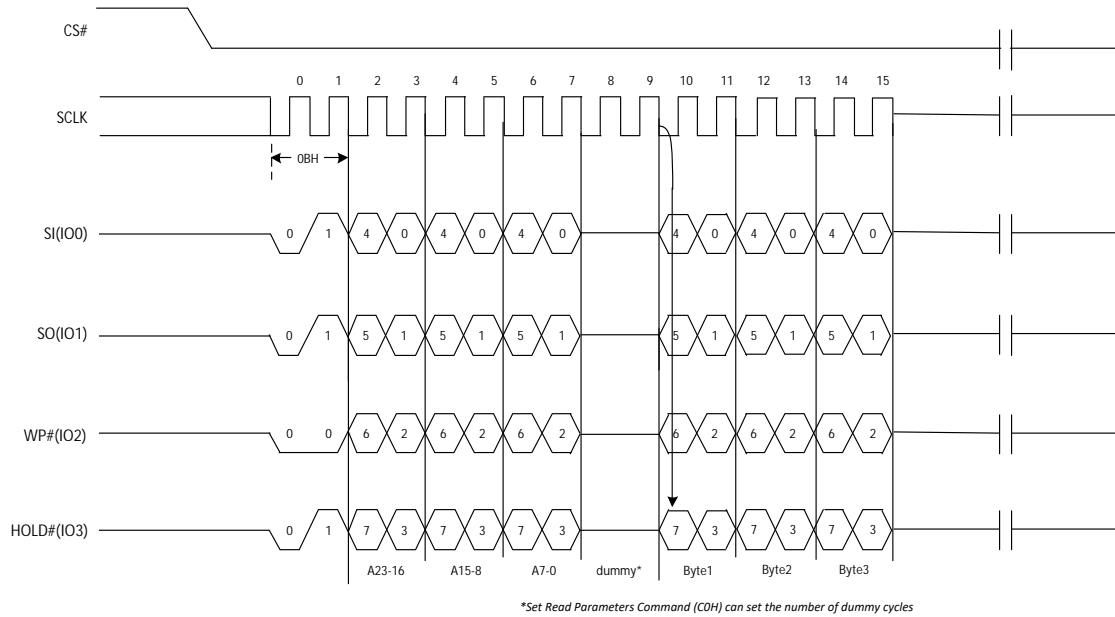
Figure 8. Read Data Bytes at Higher Speed Sequence Diagram



Fast Read (0BH) in QPI mode

The Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8. When the dummy cycle is configured to 4, addr [0] input must be 0

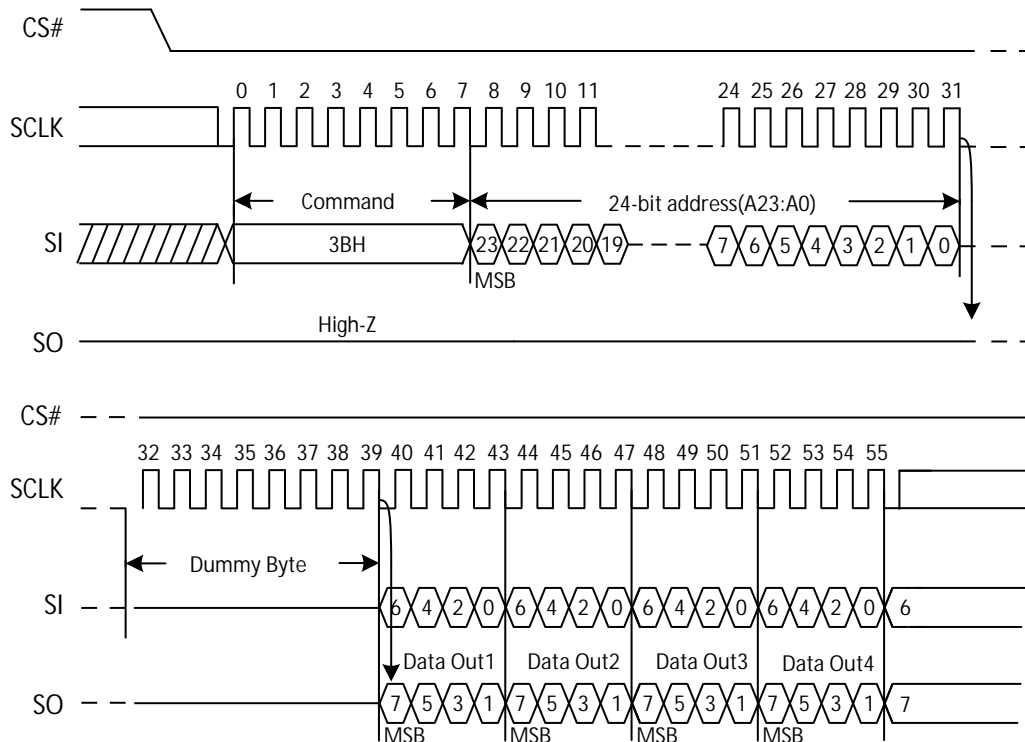
Figure 8a. Read Data Bytes at Higher Speed Sequence Diagram (QPI)



1.6.8 Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

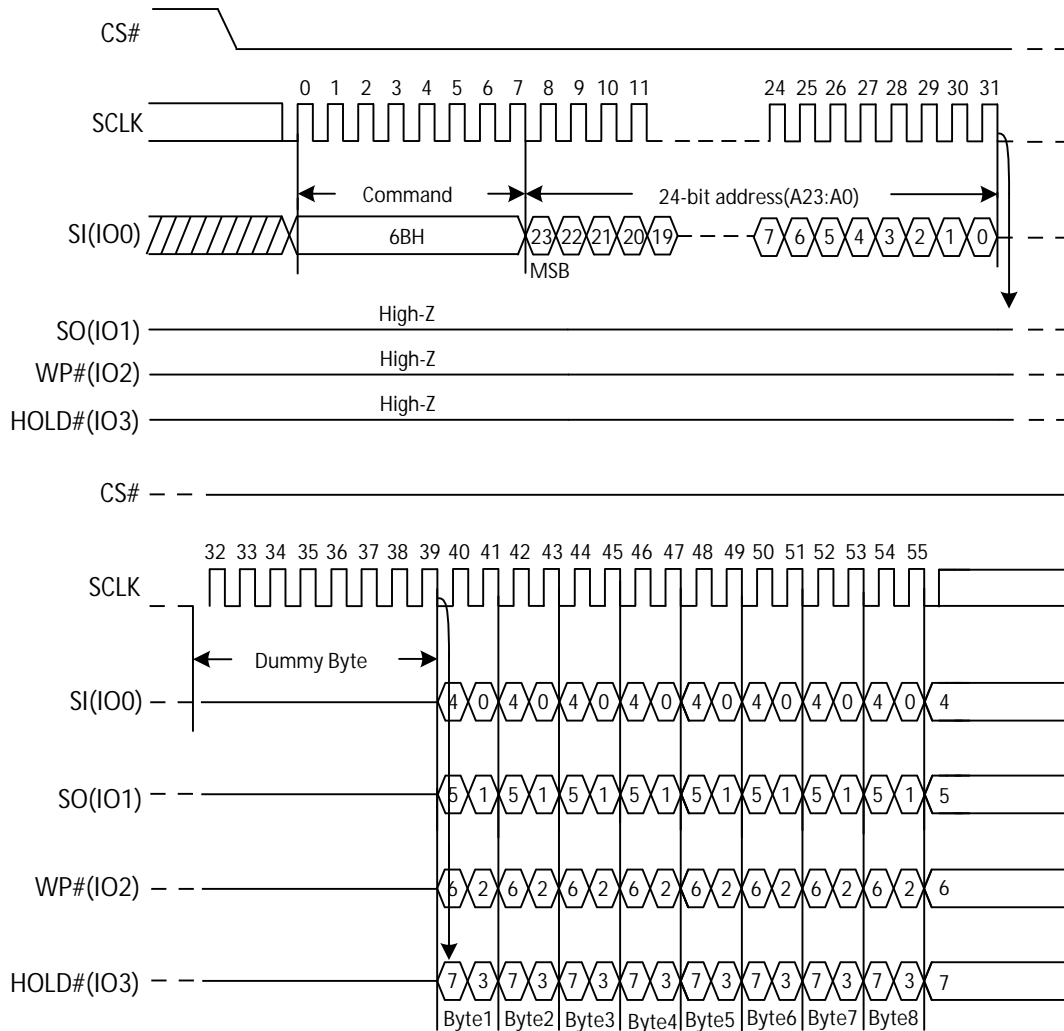
Figure 9. Dual Output Fast Read Sequence Diagram



1.6.9 Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in Figure 10. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 10. Quad Output Fast Read Sequence Diagram



1.6.10 Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 11. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Dual I/O Fast Read with "Continuous Read Mode"

The Dual I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7- 0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4)

=(1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in figure 11a. If the “Continuous Read Mode” bits (M5- 4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5- 4) before issuing normal command.

Figure 11. Dual I/O Fast Read Sequence Diagram (M5-

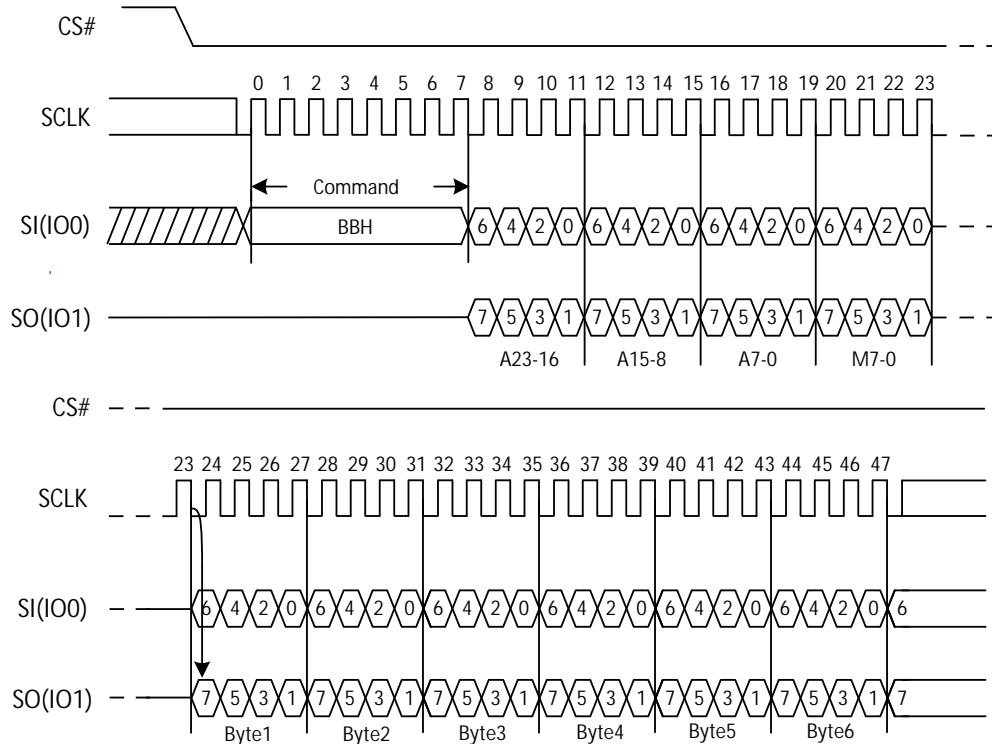
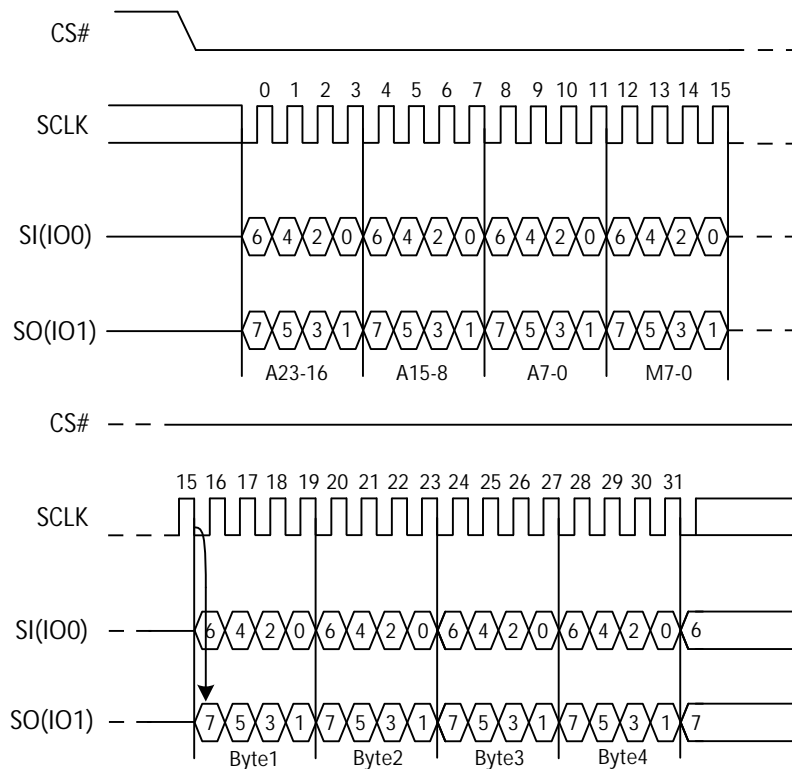


Figure 11a. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0))



1.6.11 Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in Figure 12. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5- 4) =(1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in Figure 12a. If the “Continuous Read Mode” (M5- 4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5- 4) before issuing normal command.

Figure 12. Quad I/O Fast Read Sequence Diagram (M5-

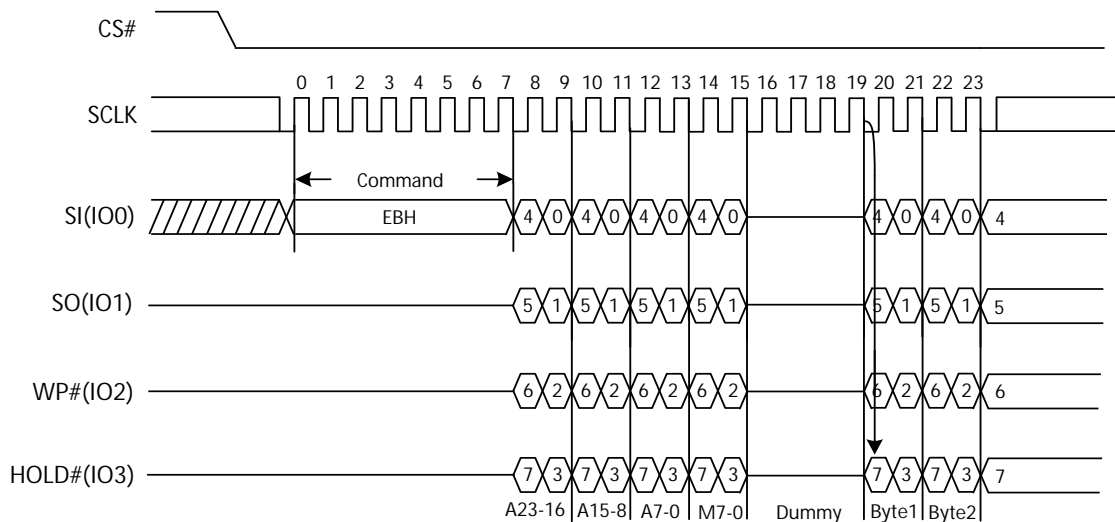
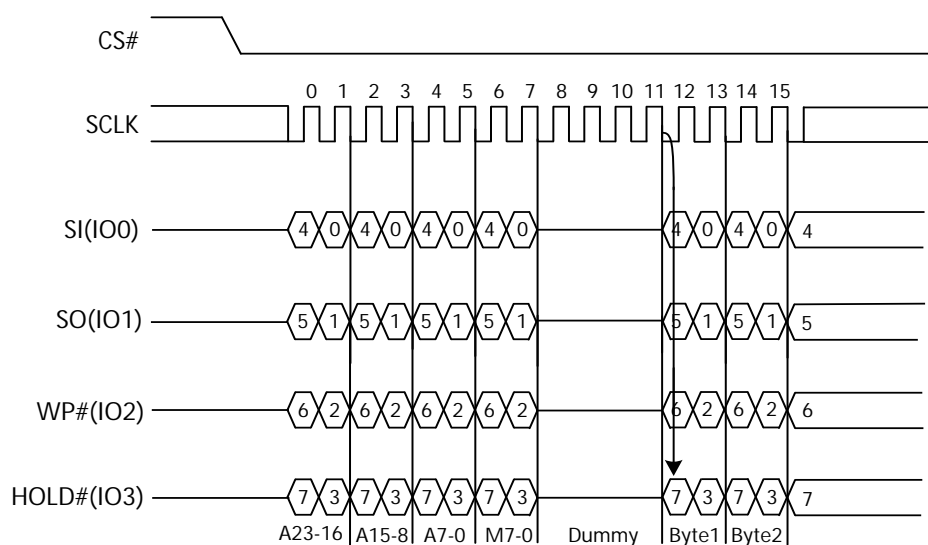


Figure 12a. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0))



Quad I/O Fast Read with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

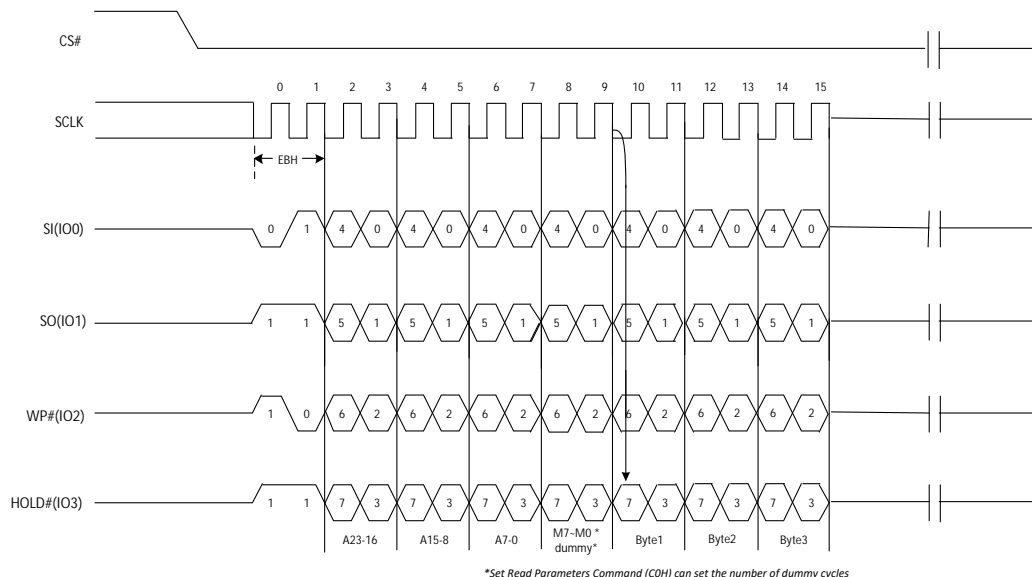
The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing “Set Burst with Wrap” (77H) commands prior to EBH. The “Set Burst with Wrap” (77H) command can either enable or disable the “Wrap Around” feature for the following EBH commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The “Set Burst with Wrap” command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

Quad I/O Fast Read (EBH) in QPI mode

The Quad I/O Fast Read command is also supported in QPI mode. See Figure12b. In QPI mode, the number of dummy clocks is configured by the “Set Read Parameters (C0H)” command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8. When the dummy cycle is configured to 4, addr[0] input must be 0. In QPI mode, the “Continuous Read Mode” bits M7-M0 are also considered as dummy clocks. “Continuous Read Mode” feature is also available in QPI mode for Quad I/O Fast Read command. “Wrap Around” feature is not available in QPI mode for Quad I/O Fast Read command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0CH) command must be used.

Figure12b. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0) QPI)



1.6.12 Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure 13. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command.

Quad I/O Word Fast Read with “Continuous Read Mode”

The Quad I/O Word Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure 13a. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the first E7H command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M7-0) before issuing normal command.

Figure 13. Quad I/O Word Fast Read Sequence Diagram (M5- 0))

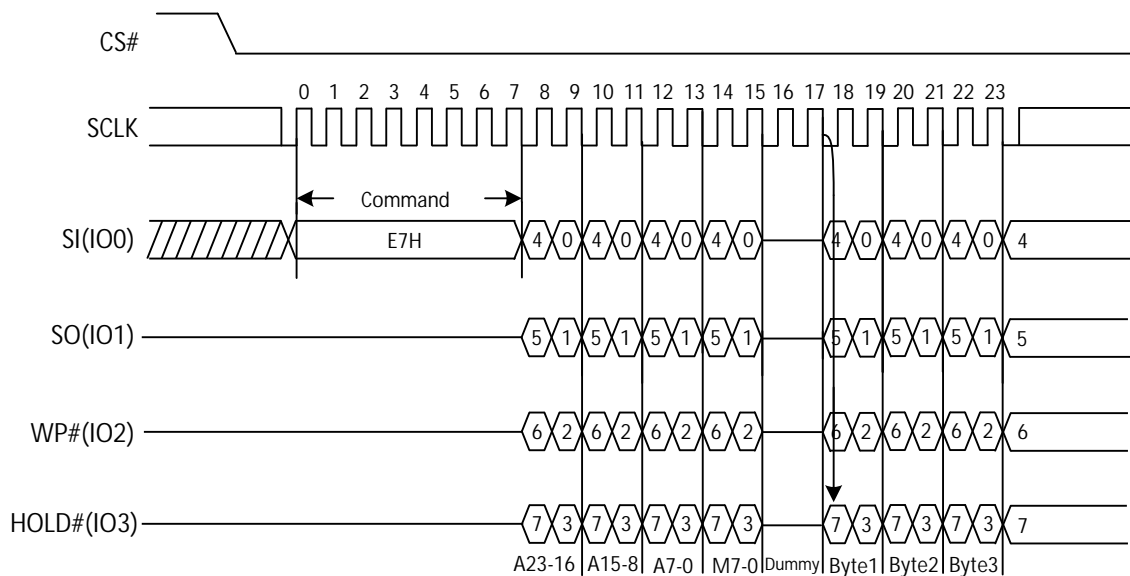
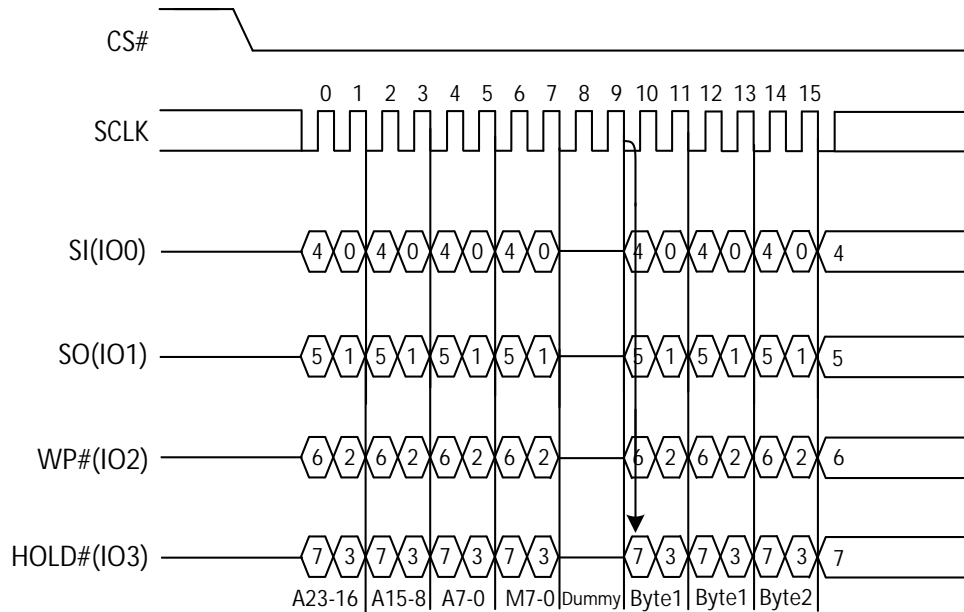


Figure13a. Quad I/O Word Fast Read Sequence Diagram (M5-4= (1, 0))


Quad I/O Word Fast Read with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The Quad I/O Word Fast Read command can be used to access a specific portion within a page by issuing “Set Burst with Wrap” (77H) commands prior to E7H. The “Set Burst with Wrap” (77H) command can either enable or disable the “Wrap Around” feature for the following E7H commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command. The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The “Set Burst with Wrap” command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

1.6.13 Set Burst with Wrap (77H)

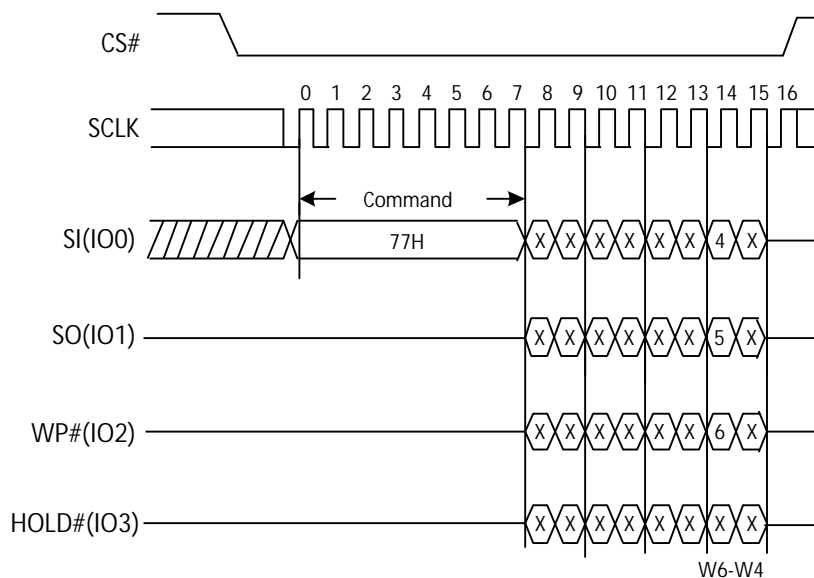
The Set Burst with Wrap command is used in conjunction with “Quad I/O Fast Read (EBH)”, “Quad I/O Word Fast Read (E7H)” and “Quad Read under DTR (EDH)” commands to access a fixed length of 8/16/32/64-byte section within a 256-byte page in standard SPI mode. The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits “Wrap bits” → CS# goes high

| W6,W5 | W4=0 | | W4=1(default) | |
|-------|-------------|-------------|---------------|-------------|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 0,0 | Yes | 8-byte | No | N/A |
| 0,1 | Yes | 16-byte | No | N/A |
| 1,0 | Yes | 32-byte | No | N/A |
| 1,1 | Yes | 64-byte | No | N/A |

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following “Quad I/O Fast Read (EBH)” and “Quad I/O Word Fast Read (E7H)” and “Quad Read under DTR (EDH)” command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

In QPI mode, the “Burst Read with Wrap (0CH)” command should be used to perform the Read Operation with “Wrap Around” feature. The Wrap Length set by W5-W6 in Standard SPI mode is still valid in QPI mode and can also be re-configured by “Set Read Parameters (C0H)” command.

Figure 14. Set Burst with Wrap Sequence Diagram



1.6.14 Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in Figure 15. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.

Figure 15. Page Program Sequence Diagram

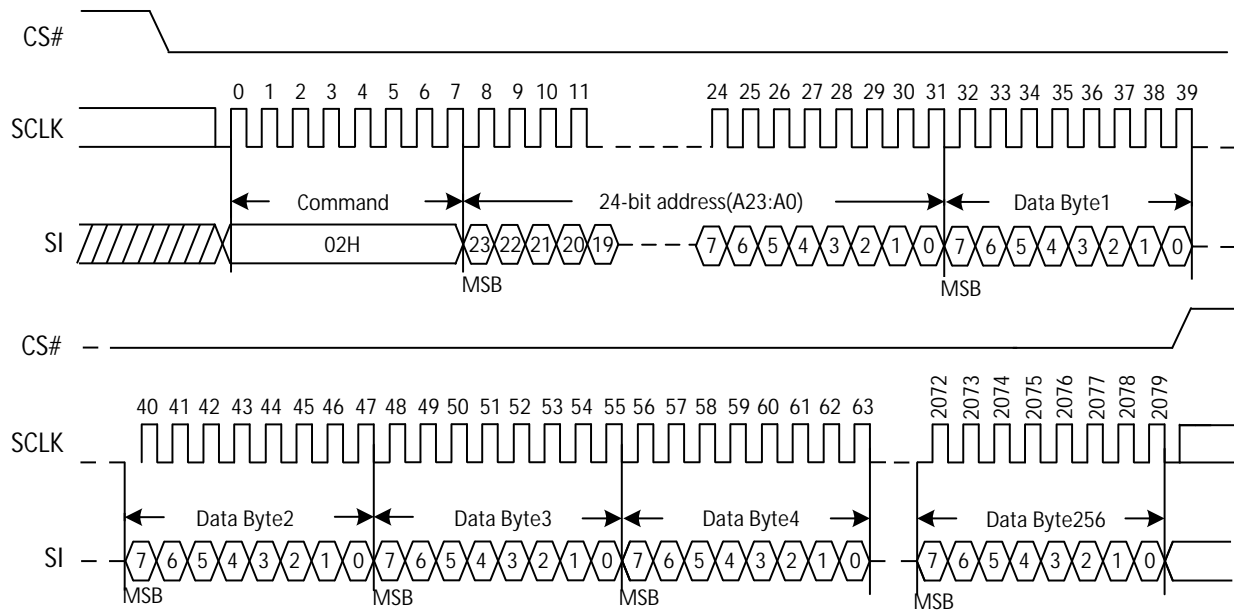
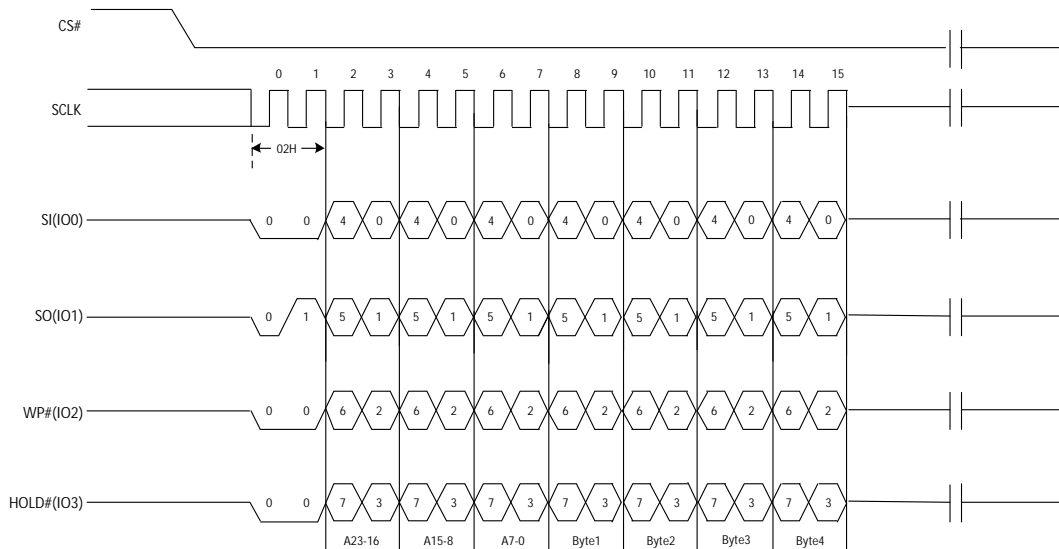


Figure15a. Page Program Sequence Diagram (QPI)



1.6.15 Quad Page Program (QPP) (32H)

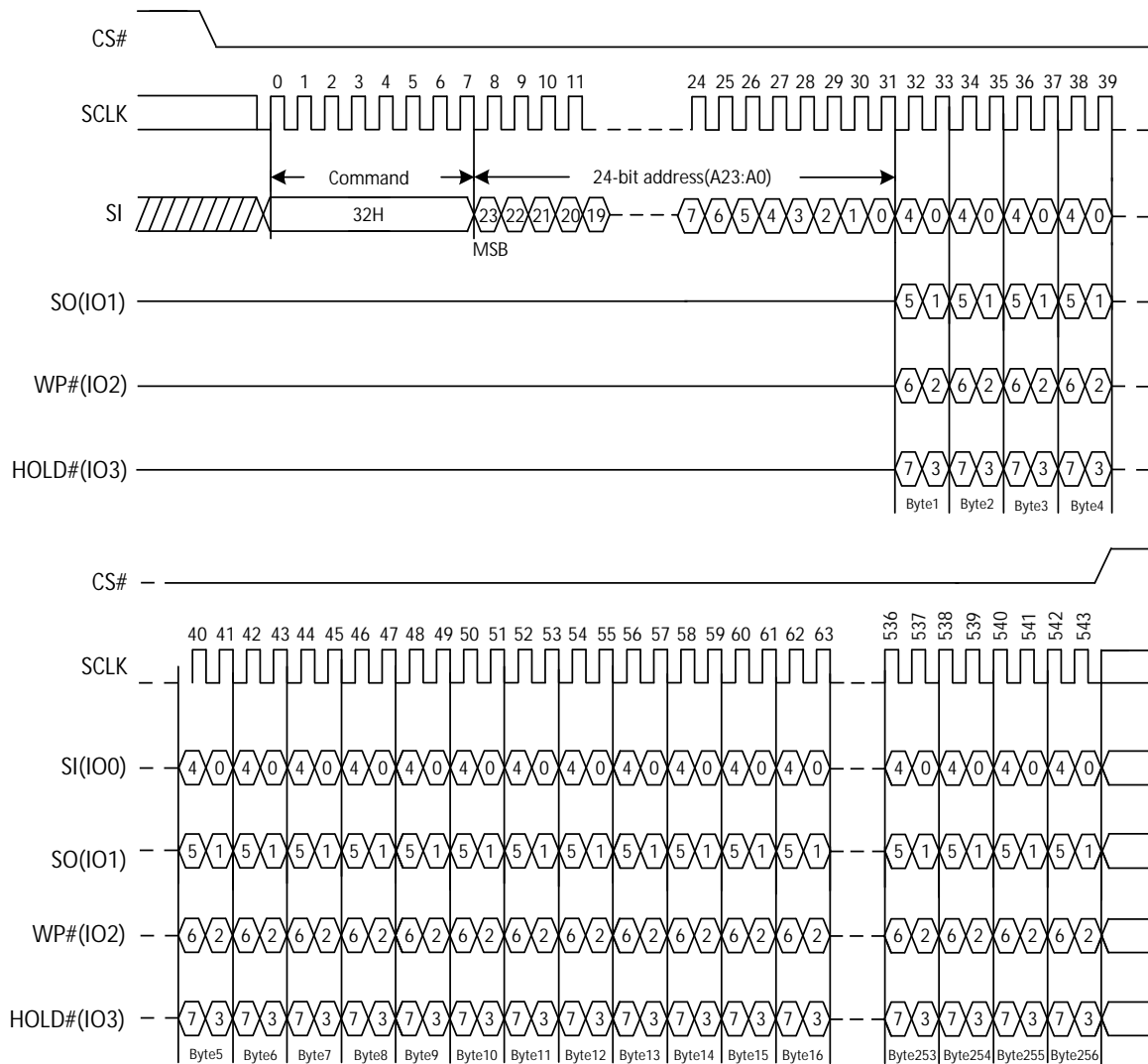
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The Quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in Figure 16. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) will not be executed.

Figure 16. Quad Page Program Sequence Diagram



1.6.16 Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 17. CS# must be driven high after the eighth

bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit (see Table 1.0 & 1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.

Figure 17. Sector Erase Sequence Diagram

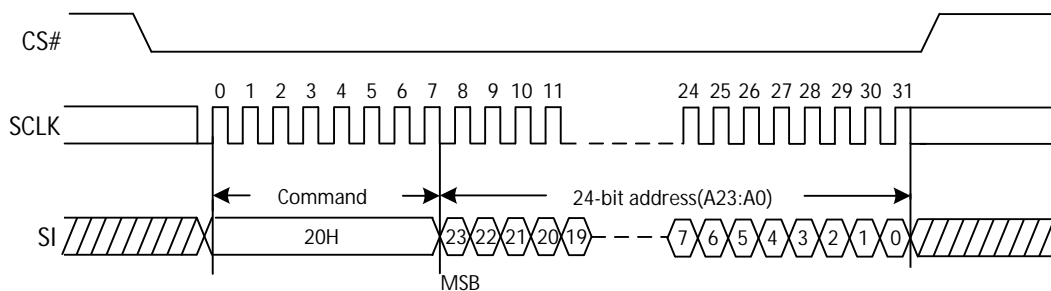
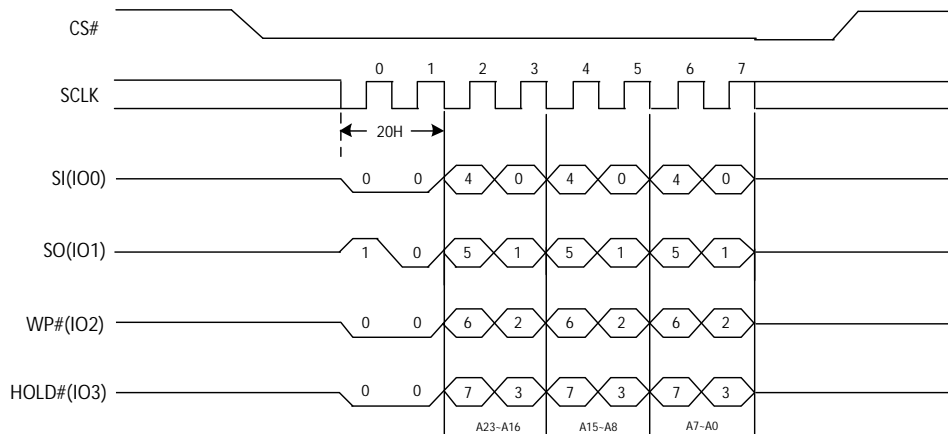


Figure 17a. Sector Erase Sequence Diagram (QPI)



1.6.17 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 18. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A

32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table 1.0 & 1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.

Figure 18. 32KB Block Erase Sequence Diagram

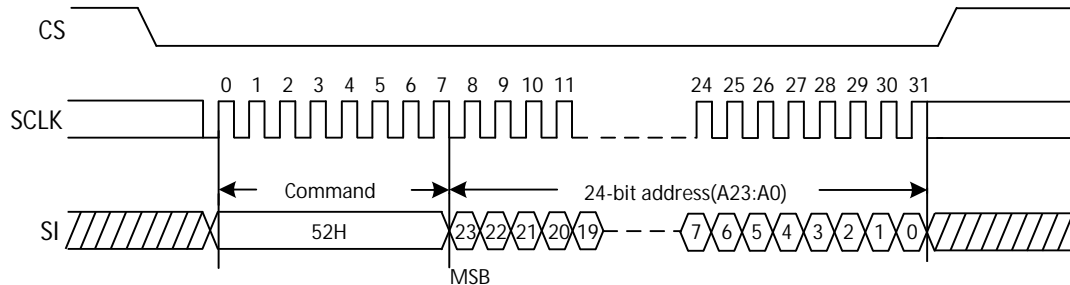
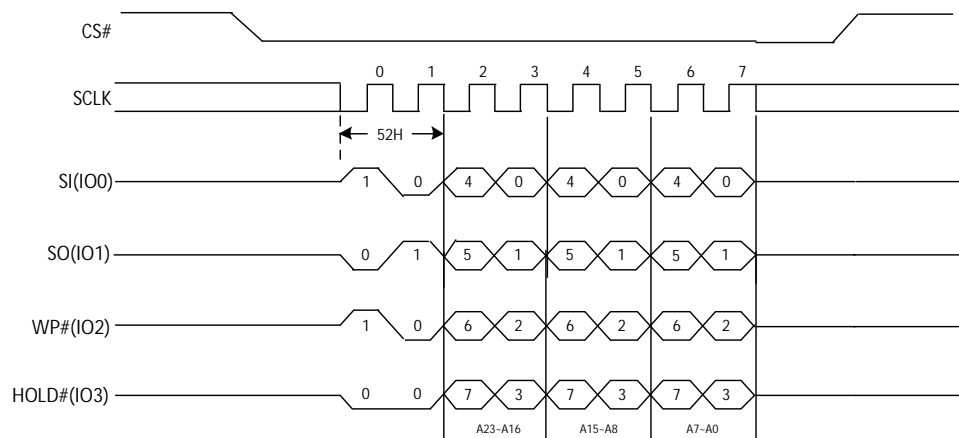


Figure 18a. 32KB Block Erase Sequence Diagram (QPI)



1.6.18 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 19. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table 1.0 & 1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.

Figure 19. 64KB Block Erase Sequence Diagram

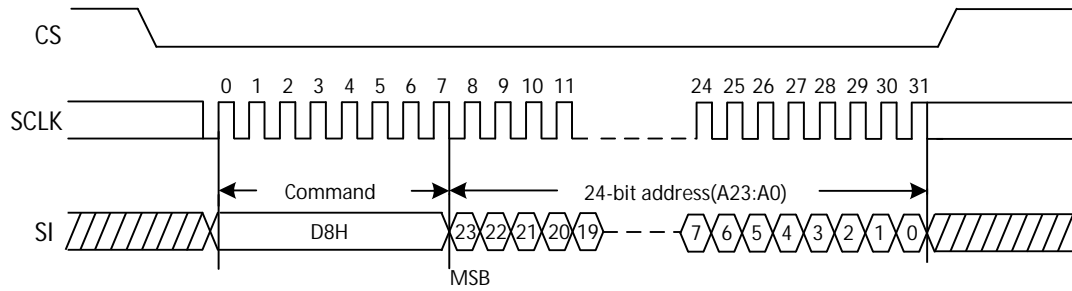
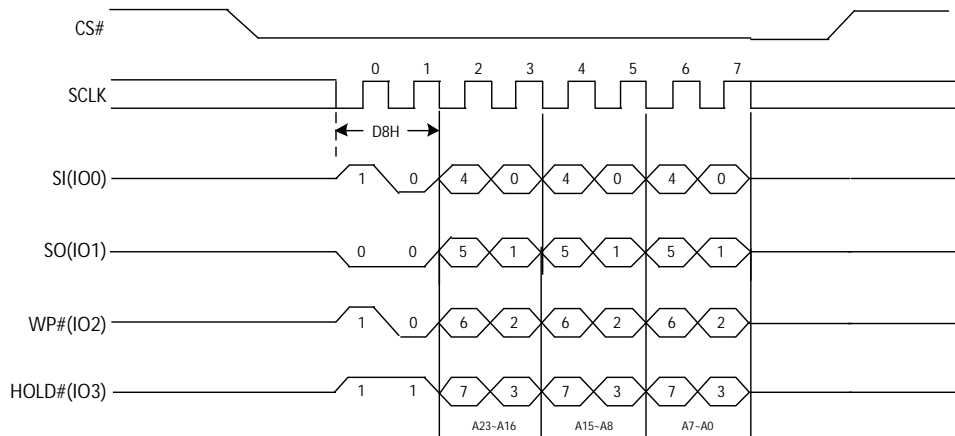


Figure19a. 64KB Block Erase Sequence Diagram (QPI)



1.6.19 Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low→sending Chip Erase command→CS# goes high. The command sequence is shown in Figure23. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or the Block Protect (BP2,BP1,and BP0)bits are 1 and CMP=1. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Note: Power disruption during erase operation will cause incomplete erase, thus recommend to perform a re-erase once power resume.

Figure 20. Chip Erase Sequence Diagram

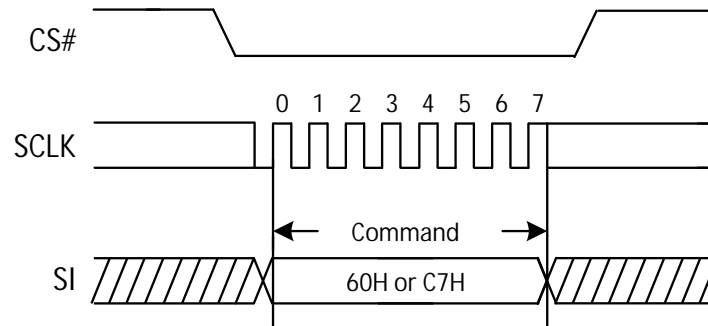
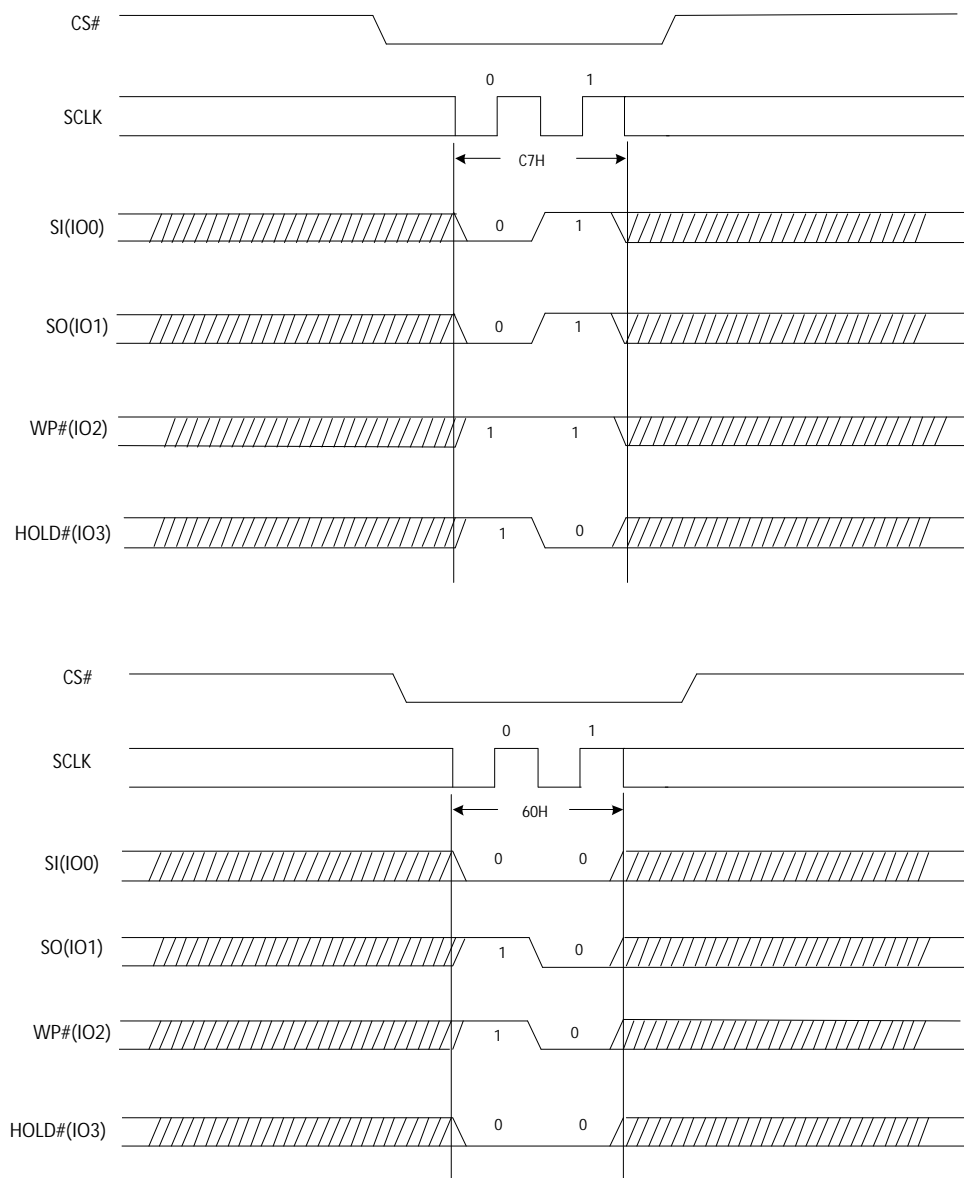


Figure20a. Chip Erase Sequence Diagram (QPI)



1.6.20 Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. The command sequence is shown in Figure 21. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 21. Deep Power-Down Sequence Diagram

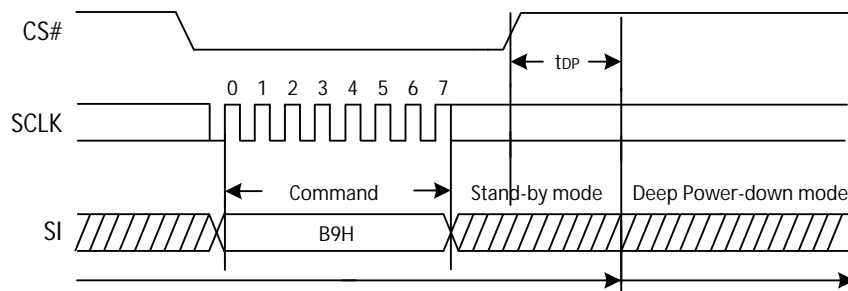
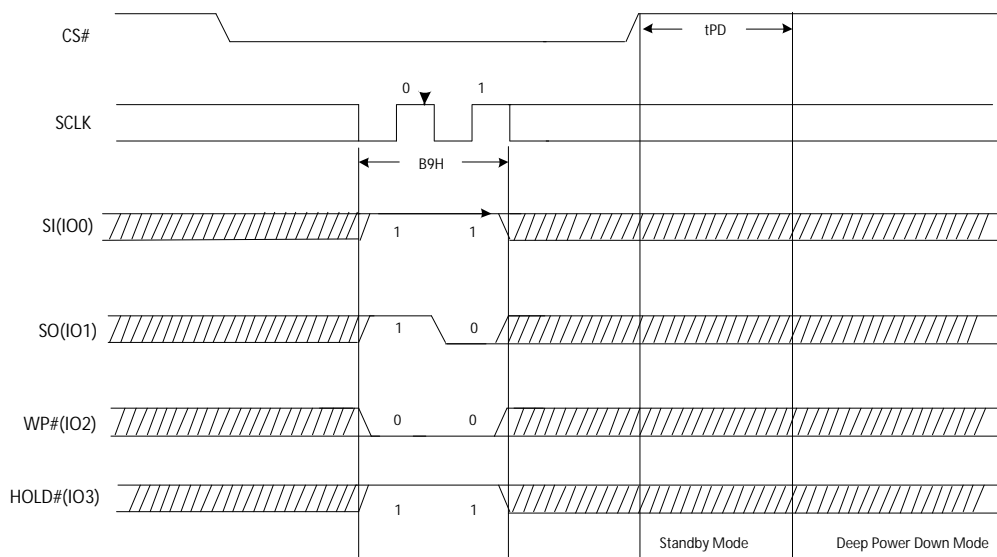


Figure 21a. Deep Power-Down Sequence Diagram (QPI)



1.6.21 Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read/Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown in Figure22. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure22b. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 22b, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down/Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not effects on the current cycle.

Figure 22. Release Power-Down Sequence Diagram

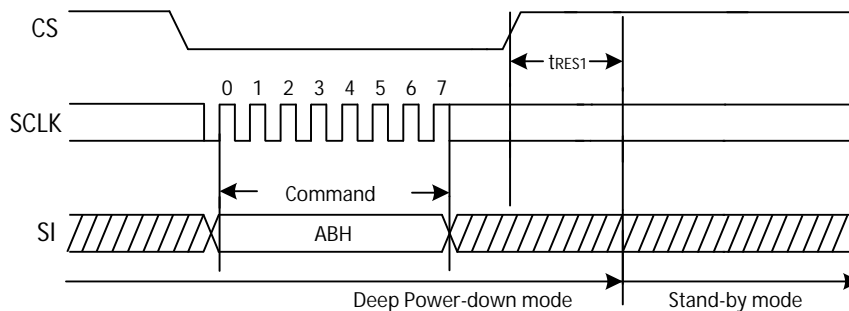


Figure 22a. Release Power-Down Sequence Diagram (QPI)

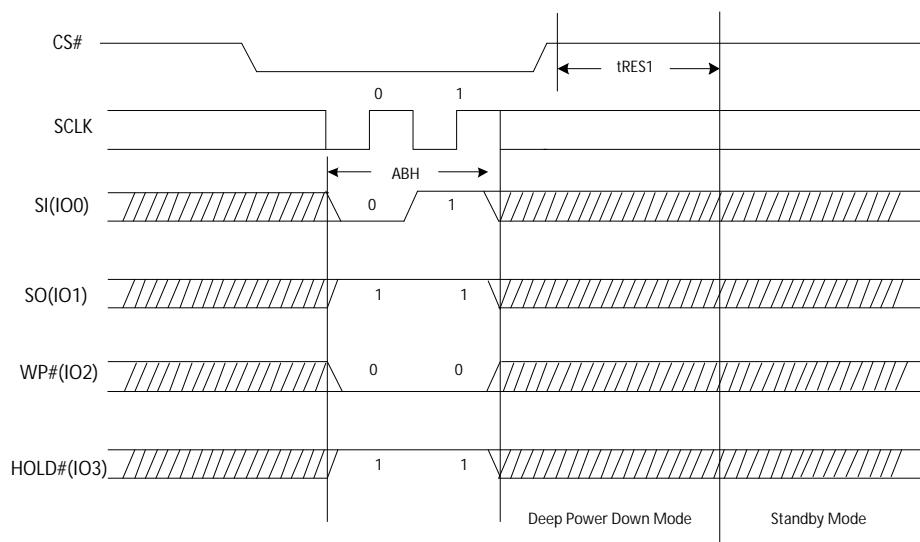


Figure 22b. Release Power-Down/Read Device ID Sequence Diagram

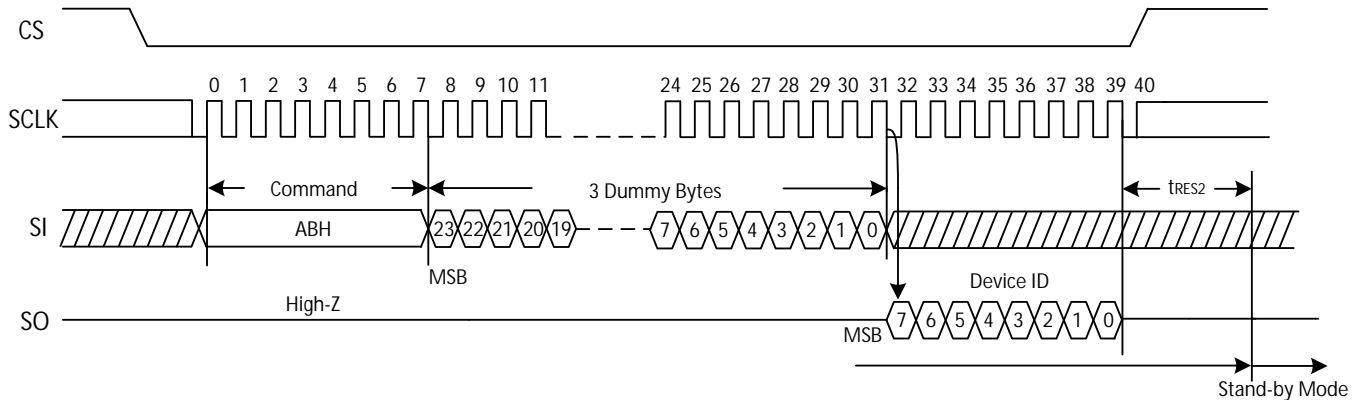
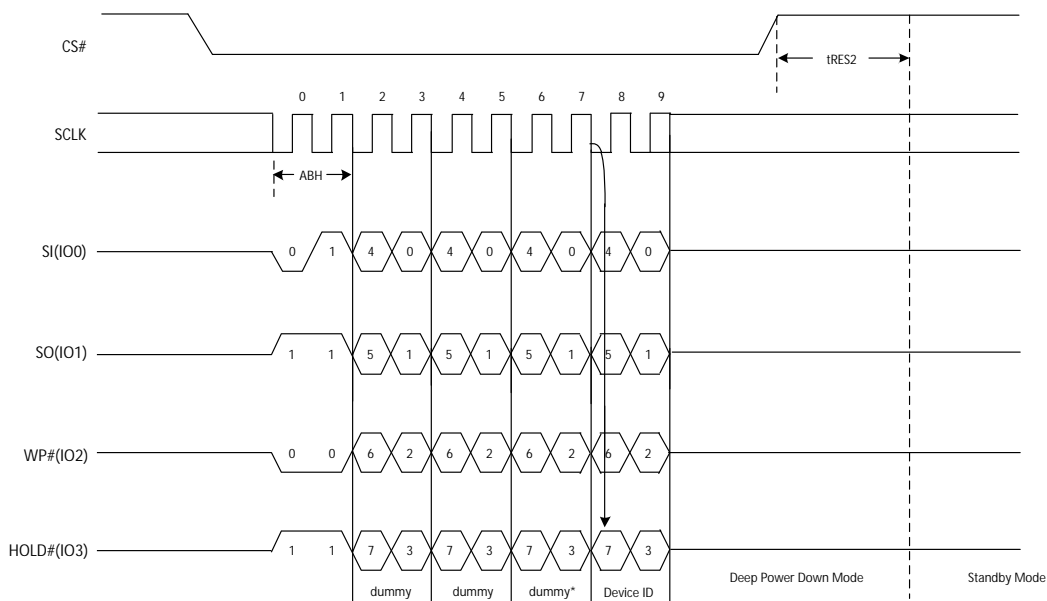


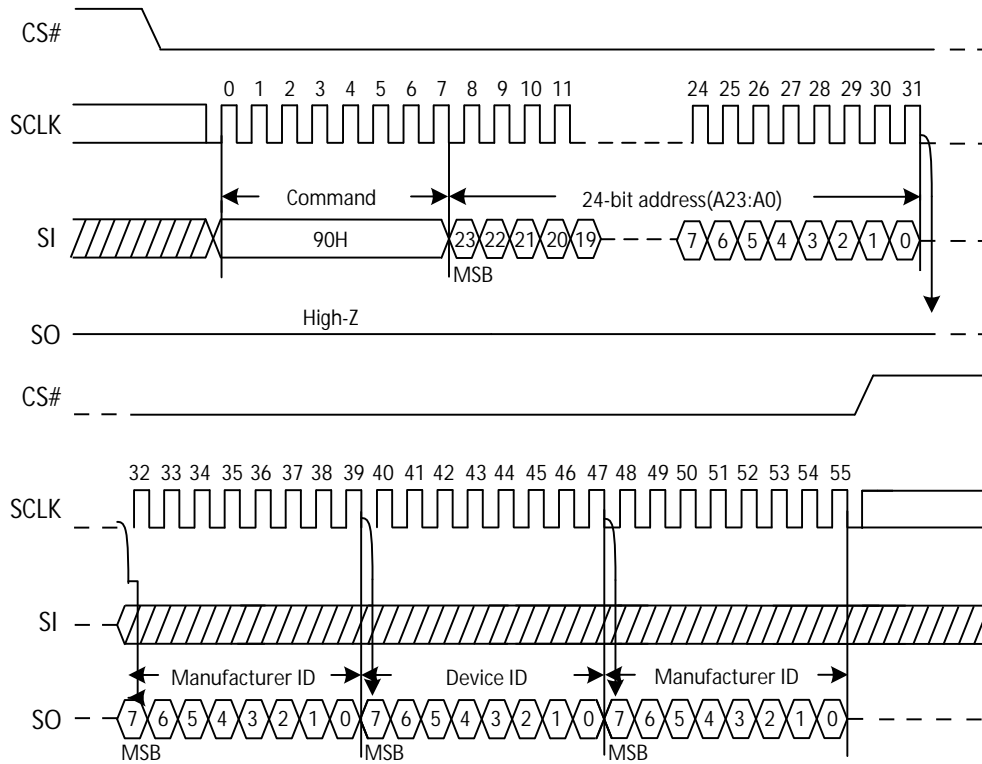
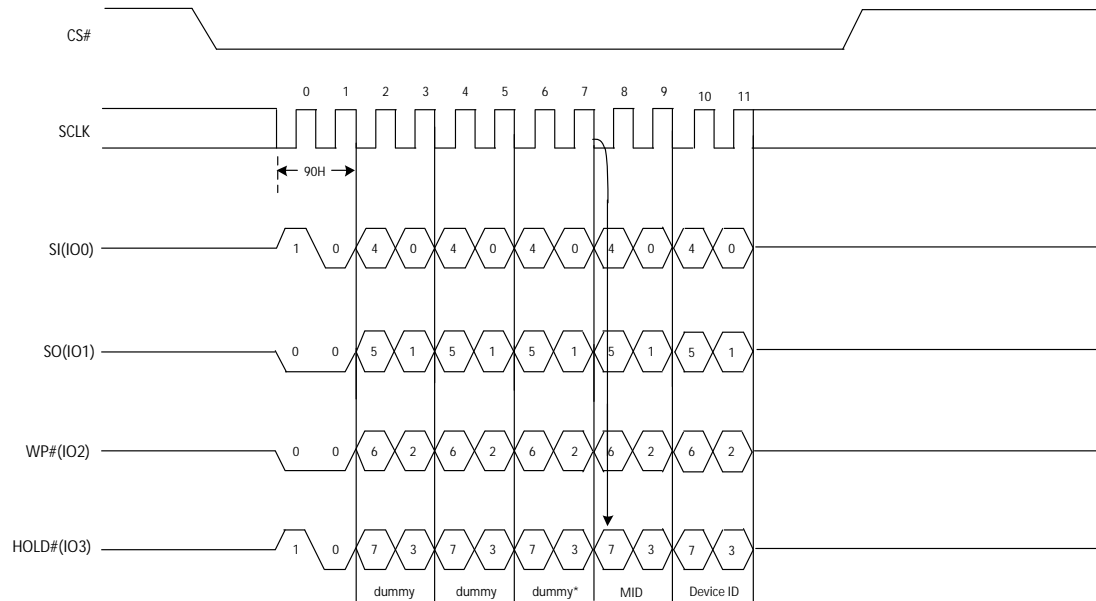
Figure 22c. Release Power-Down/Read Device ID Sequence Diagram (QPI)



1.6.22 Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in Figure 23. If the 24-bit address is initially set to 000001H, the Device ID will be read first. In QPI mode the dummy cycles can be configured by C0H command. When the dummy cycle is configured to 4, addr [0] input must be 0.

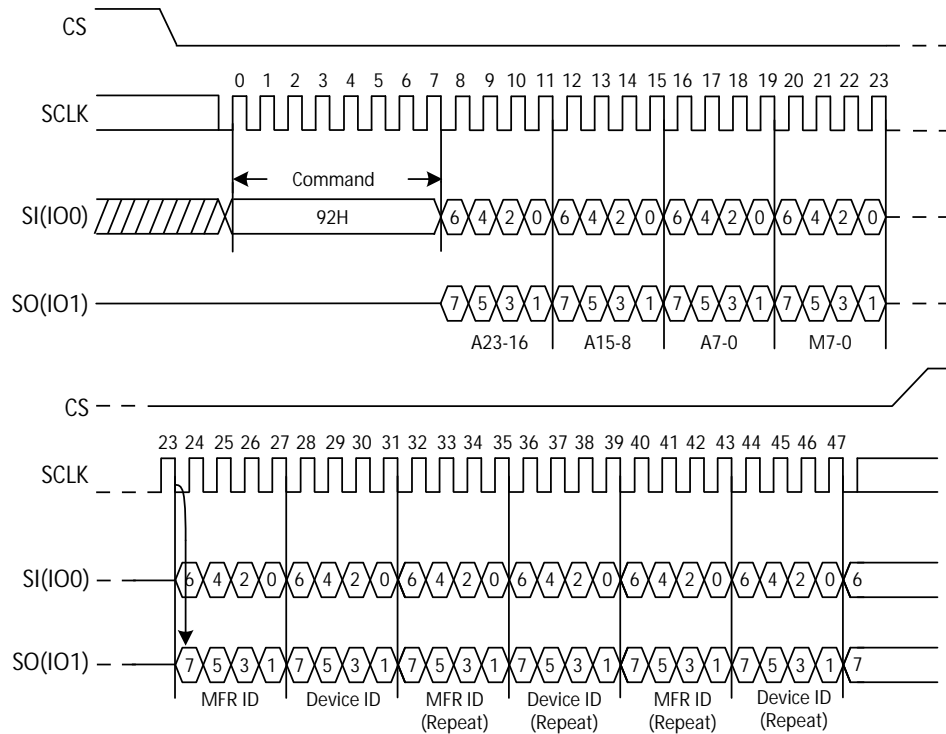
Figure 23. Read Manufacture ID/ Device ID Sequence Diagram

Figure 23a. Read Manufacture ID/ Device ID Sequence Diagram (QPI)


1.6.23 Read Manufacture ID/ Device ID Dual I/O (92H)

The Read Manufacturer/Device ID Dual I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the CS# pin low and shifting the command code "92H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 24. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 24. Read Manufacture ID/ Device ID Dual I/O Sequence Diagram



1.6.24 Read Manufacture ID/ Device ID Quad I/O (94H)

The Read Manufacturer/Device ID Quad I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The command is initiated by driving the CS# pin low and shifting the command code "94H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 25. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

The timing diagram shows the following signals and data flow:

- CS:** Chip Select, active-low, goes low at cycle 0 and returns high at cycle 32.
- SCLK:** Serial Clock, provided by the host, with 32 cycles shown.
- SI(IO0):** Serial Input. A shaded area indicates the host driving the signal. A command '94H' is sent from the host to the device between cycles 1 and 7. Data is received from the device starting at cycle 8.
- SO(IO1):** Serial Output. Data is sent from the device to the host starting at cycle 8.
- WP#(IO2):** Write Protect, active-low, goes low at cycle 8 and remains low.
- HOLD#(IO3):** Hold, active-low, goes low at cycle 8 and remains low.

The data is organized into 8-bit bytes, with labels indicating the data source:

- A23-16:** Address data from A23 to A16.
- A15-8:** Address data from A15 to A8.
- A7-0:** Address data from A7 to A0.
- M7-0:** Memory data from M7 to M0.
- Dummy:** Dummy data.
- MID:** Memory ID.
- DID:** Data ID.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure26. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

1.6.26 Erase Security Registers (44H)

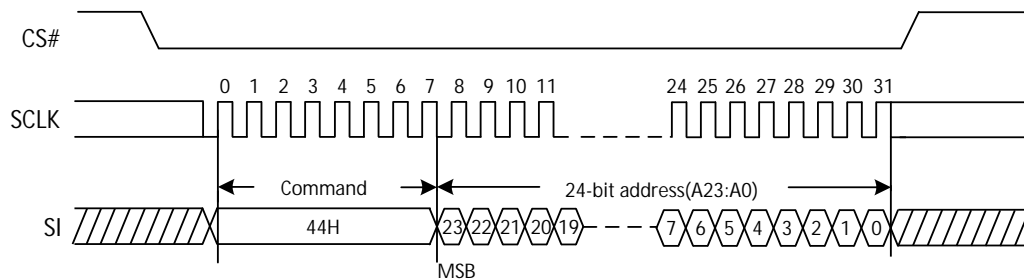
The device provides four 256-byte Security Registers which only erased all at once but able to program individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers Command → CS# goes high. The command sequence is shown in Figure 29. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

| Address | A23-A16 | A15-A10 | A9-A0 |
|--------------------|----------|---------|------------|
| Security Registers | 00000000 | 000000 | Don't Care |

Figure 29. Erase Security Registers command Sequence Diagram



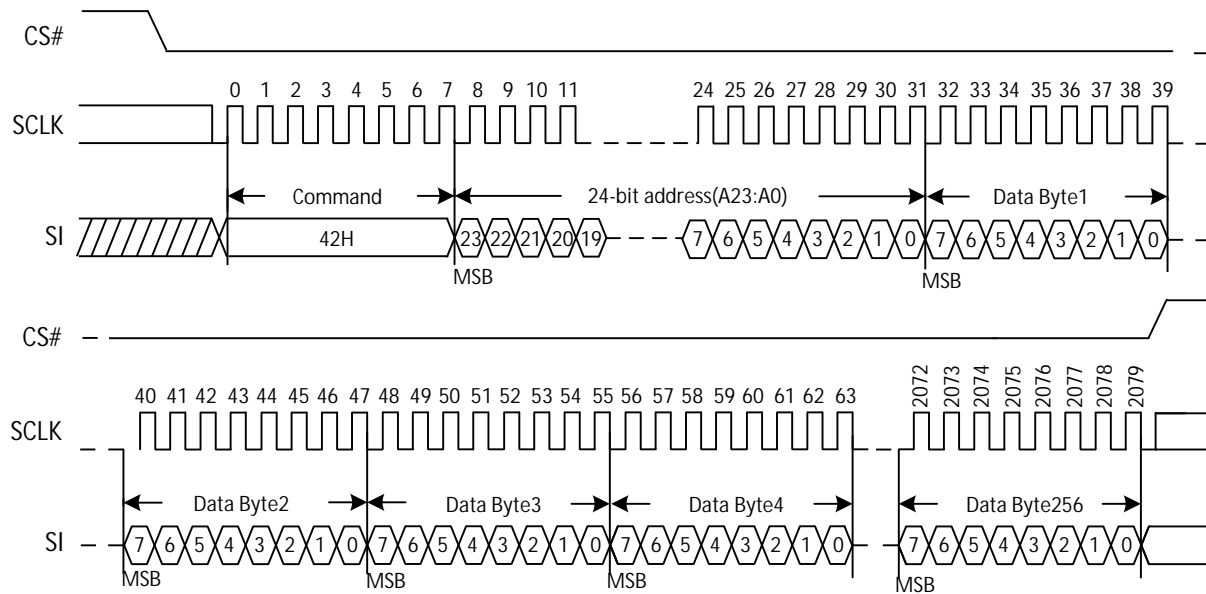
1.6.27 Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

| Address | A23-A16 | A15-A8 | A7-A0 |
|----------------------|---------|--------|--------------|
| Security Registers 0 | 00H | 00H | Byte Address |
| Security Registers 1 | 00H | 01H | Byte Address |
| Security Registers 2 | 00H | 02H | Byte Address |
| Security Registers 3 | 00H | 03H | Byte Address |

Figure 30. Program Security Registers command Sequence Diagram

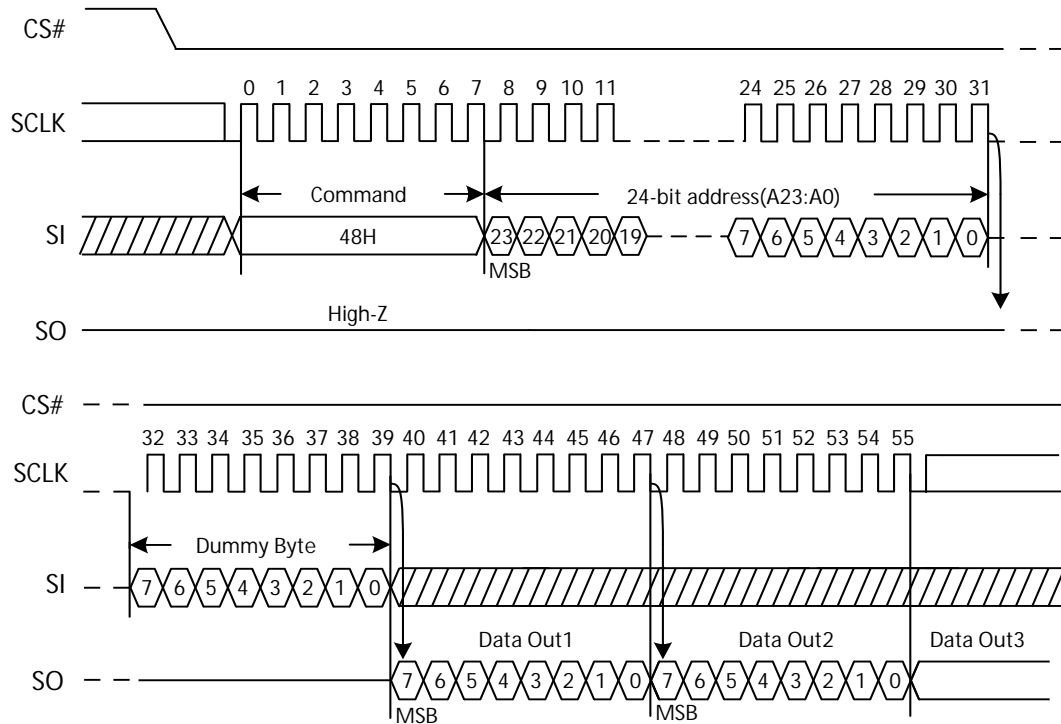


1.6.28 Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C , during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

| Address | A23-A16 | A15-A10 | A9-A0 |
|--------------------|----------|---------|---------|
| Security Registers | 00000000 | 000000 | Address |

Figure 31. Read Security Registers command Sequence Diagram



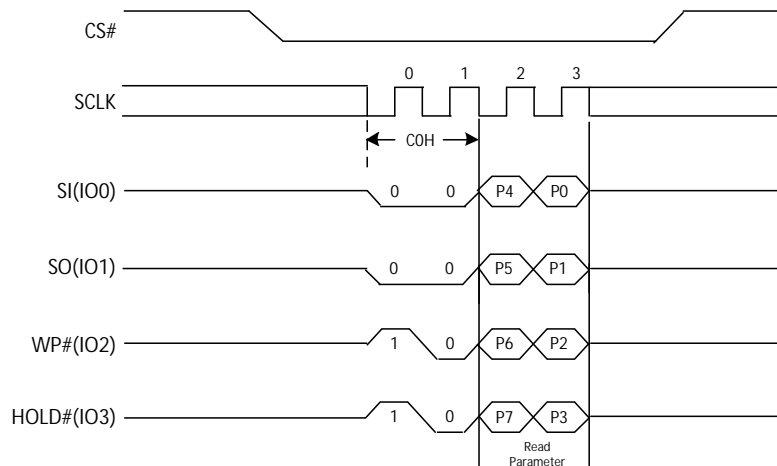
1.6.29 Set Read Parameters (C0H)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read-frequency or minimum data access latency, "Set Read Parameters (C0H)" instruction can be used to configure the number of dummy clocks for "Fast Read (0BH)", "Fast Read Quad I/O (EBH)" & "Burst Read with Wrap (0CH)" instructions, and to configure the number of bytes of "Wrap Length" for the "Burst Read with Wrap (0CH)" instruction. In Standard SPI mode, the "Set Read Parameters (C0h)" instruction is not accepted.

The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed and will remain unchanged when the device is switched from Standard SPI mode to QPI mode and requires to be set again, prior to any 0Bh, EBh or 0Ch instructions. When the device is switched from QPI mode to SPI mode, the number of dummy clocks goes back to default.

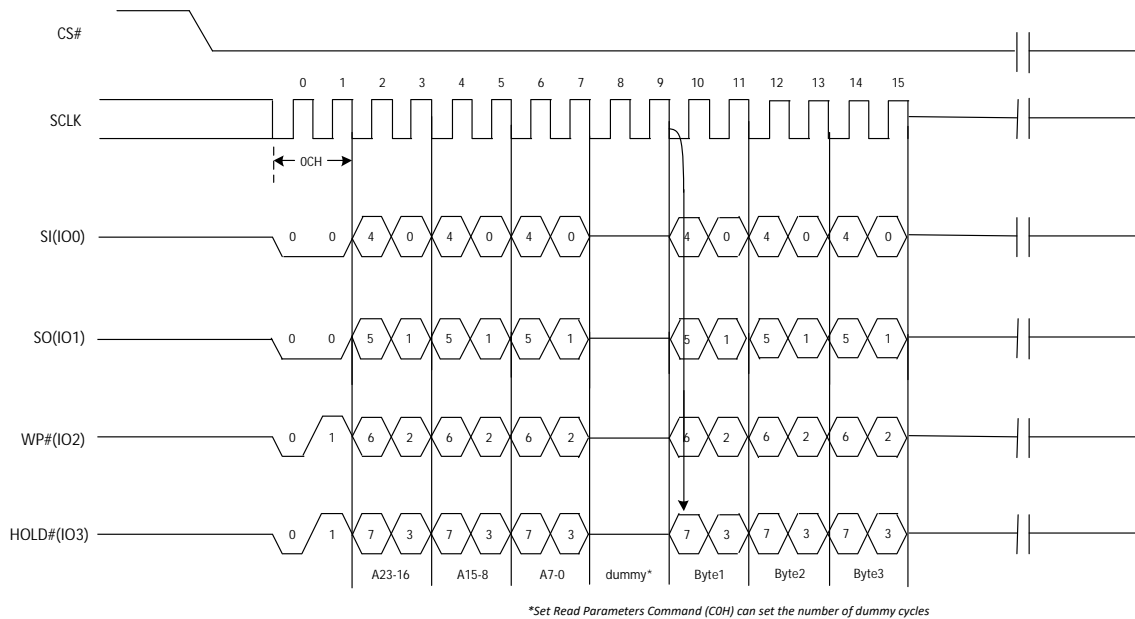
The default "Wrap Length" after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 8. The "Wrap Length" is set by W6-4 bit in the "Set Burst with Wrap (77h)" instruction in Standard SPI mode and by P1-P0 in the "Set Read Parameters (C0H)" in the QPI mode. The Wrap Length set by P1-P0 in QPI mode is still valid in SPI mode and can also be re-configured by "Set Burst with Wrap (77h)".

| P5-P4 | Dummy Clocks | Maximum Read Freq. | P1-P0 | Wrap Length |
|-------|--------------|--------------------|-------|-------------|
| 0 0 | 4 | 48MHz | 0 0 | 8-byte |
| 0 1 | 4 | 48MHz | 0 1 | 16-byte |
| 1 0 | 6 | 48MHz | 1 0 | 32-byte |
| 1 1 | 8 | 48MHz | 1 1 | 64-byte |

Figure32. Set Read Parameters command Sequence Diagram


1.6.30 Burst Read with Wrap (0CH)

The "Burst Read with Wrap (0CH)" command provides an alternative way to perform the read operation with "Wrap Around" in QPI mode. This command is similar to the "Fast Read (0BH)" command in QPI mode, except the addressing of the read operation will "Wrap Around" to the beginning boundary of the "Wrap Around" once the ending boundary is reached. The "Wrap Length" and the number of dummy clocks can be configured by the "Set Read Parameters (C0H)" command.

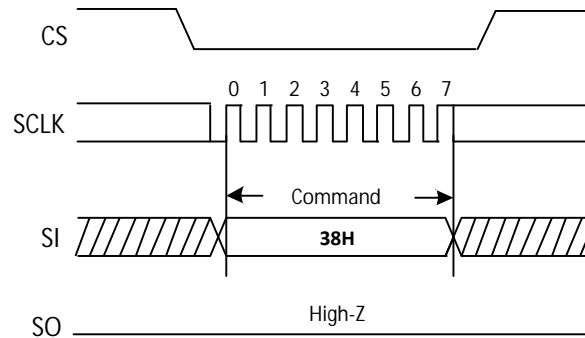
Figure 33. Burst Read with Wrap command Sequence Diagram


*Set Read Parameters Command (C0H) can set the number of dummy cycles

1.6.31 Enable QPI (38H)

The device support both Standard/Dual/Quad SPI and QPI mode. The "Enable QPI (38H)" command can switch the device from SPI mode to QPI mode. See the command Table 2a for all support QPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-1 must be set to 1 first, and "Enable QPI (38H)" command must be issued. If the QE bit is 0, the "Enable QPI (38H)" command will be ignored and the device will remain in SPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged.

Figure 34. Enable QPI mode command Sequence Diagram

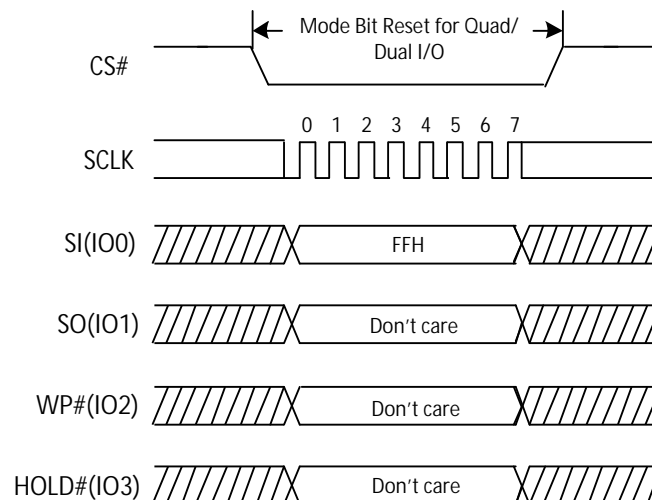


1.6.32 Continuous Read Mode Reset (CRMR) (FFH)/ Disable QPI (FFH)

The Dual/Quad I/O Fast Read operations, “Continuous Read Mode” bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH/E7H command code.

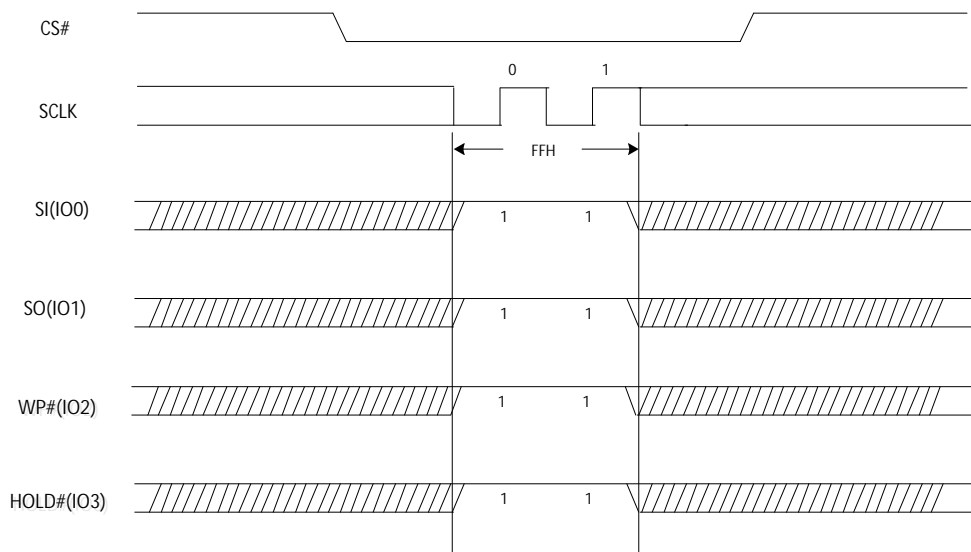
Because the device has no hardware reset pin, so if Continuous Read Mode bits are set to “AXH”, the device will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the “AXH” state and allow standard SPI command to be recognized. The command sequence is show in Figure35.

Figure 35. Continuous Read Mode Reset Sequence Diagram



Disable QPI (FFH)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, the “Disable QPI (FFH)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged. When the device is in QPI mode, the first FFH command will exit continuous read mode and the second FFH command will exit QPI mode.

Figure 35a. Disable QPI mode command Sequence Diagram


1.6.33 Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Read Parameter setting (P7-P0) and Wrap Bit Setting (W6-W4).

The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST_R to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

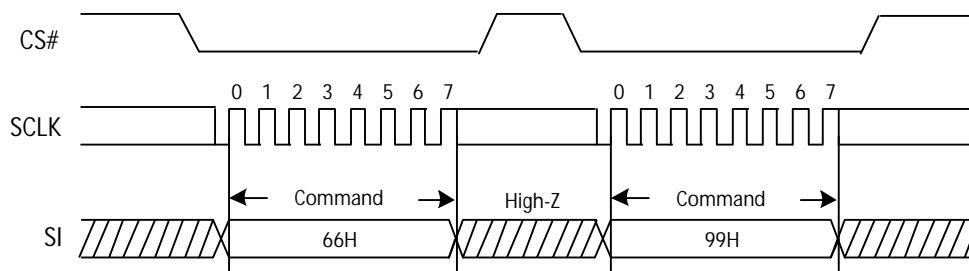
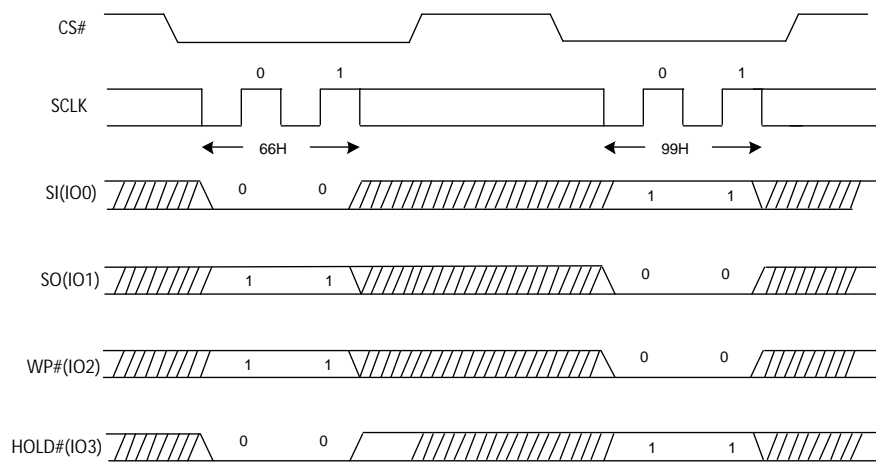
Figure 36. Enable Reset and Reset command Sequence Diagram


Figure 36a. Enable Reset and Reset command Sequence Diagram (QPI)


1.6.34 Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

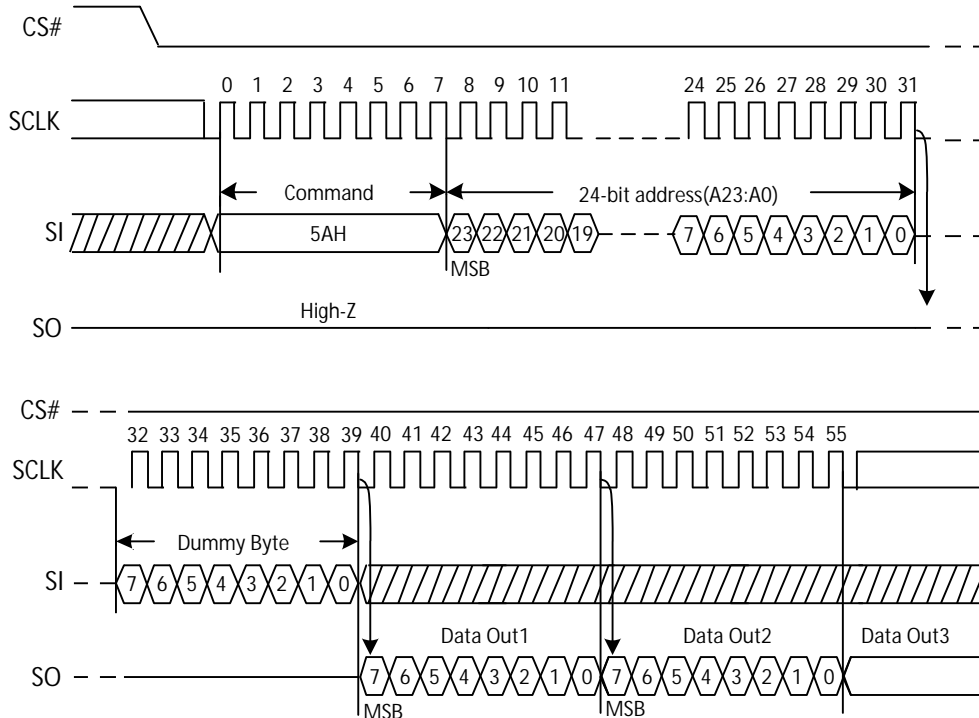
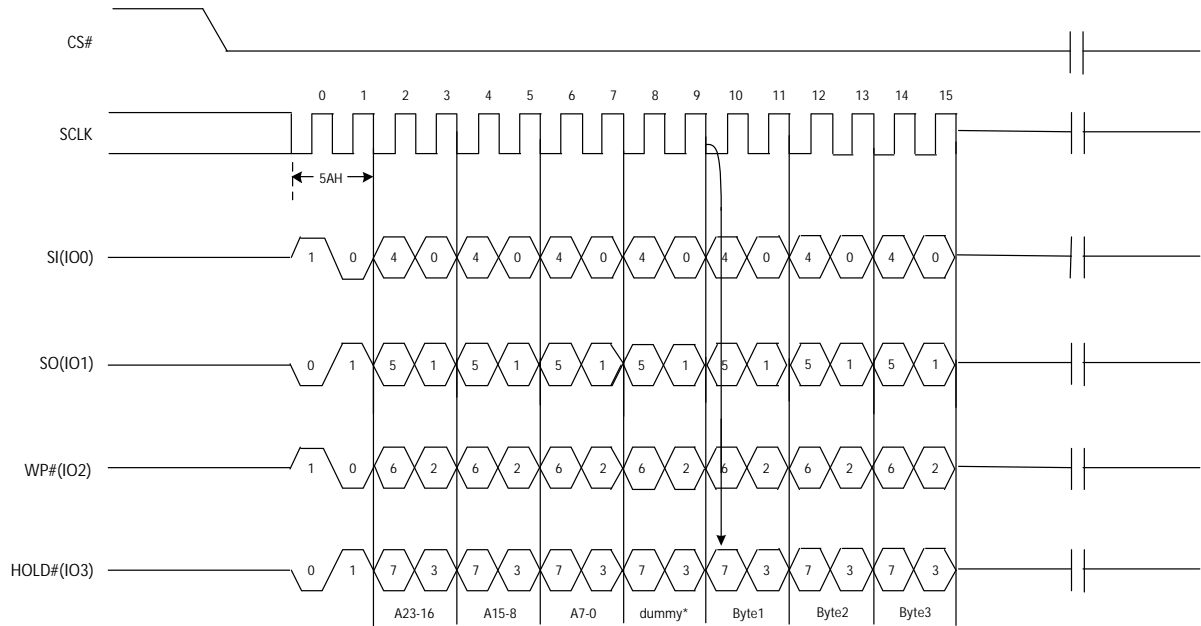
Figure 37. Read Serial Flash Discoverable Parameter command Sequence Diagram


Figure 37a. Read Serial Flash Discoverable Parameter command Sequence Diagram (QPI)


1.6.35 Read Unique ID (5AH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command → 00H → 01H → 94H → Dummy byte → 128bit Unique ID Out → CS# goes high.

The command sequence is show below.

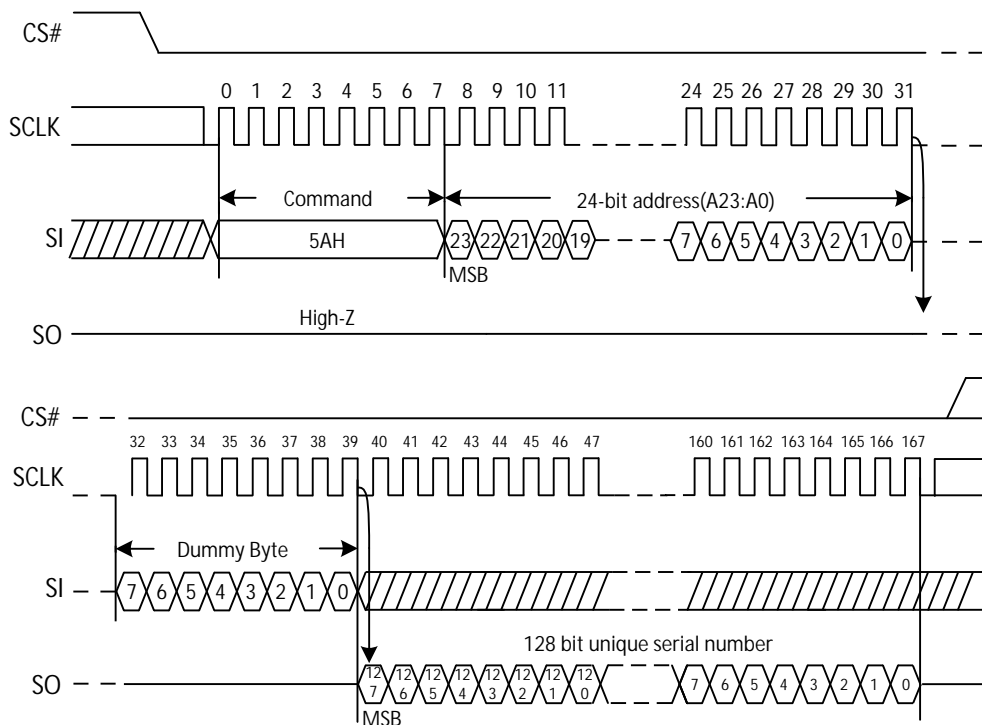
Figure 38. Read Unique ID (RUID) Sequence (Command 5AH)


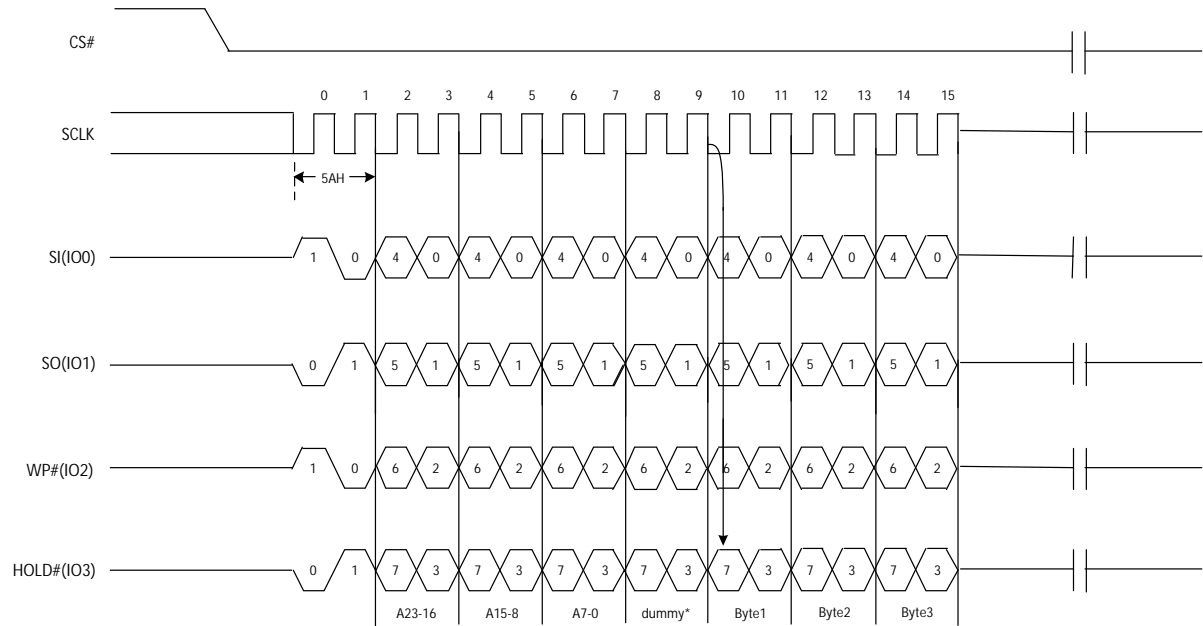
Figure 38a. Read Serial Flash Discoverable Parameter command Sequence Diagram (QPI)


Table 3. Signature and Parameter Identification Data Values

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|--|--|------------------|-----------------|------|------|
| SFDP Signature | Fixed:50444653H | 00H | 07:00 | 53H | 53H |
| | | 01H | 15:08 | 46H | 46H |
| | | 02H | 23:16 | 44H | 44H |
| | | 03H | 31:24 | 50H | 50H |
| SFDP Minor Revision Number | Start from 00H | 04H | 07:00 | 00H | 00H |
| SFDP Major Revision Number | Start from 01H | 05H | 15:08 | 01H | 01H |
| Number of Parameters Headers | Start from 00H | 06H | 23:16 | 01H | 01H |
| Unused | Contains 0xFFH and can never be changed | 07H | 31:24 | FFH | FFH |
| ID number (JEDEC) | 00H: It indicates a JEDEC specified header | 08H | 07:00 | 00H | 00H |
| Parameter Table Minor Revision Number | Start from 0x00H | 09H | 15:08 | 00H | 00H |
| Parameter Table Major Revision Number | Start from 0x01H | 0AH | 23:16 | 01H | 01H |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 0BH | 31:24 | 09H | 09H |
| Parameter Table Pointer (PTP) | First address of JEDEC Flash Parameter table | 0CH | 07:00 | 30H | 30H |
| | | 0DH | 15:08 | 00H | 00H |
| | | 0EH | 23:16 | 00H | 00H |
| Unused | Contains 0xFFH and can never be changed | 0FH | 31:24 | FFH | FFH |
| ID Number(XTX Manufacturer ID) | It is indicates XTX manufacturer ID | 10H | 07:00 | 0BH | 0BH |
| Parameter Table Minor Revision Number | Start from 0x00H | 11H | 15:08 | 00H | 00H |
| Parameter Table Major Revision Number | Start from 0x01H | 12H | 23:16 | 01H | 01H |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 13H | 31:24 | 03H | 03H |
| Parameter Table Pointer (PTP) | First address of XTX Flash Parameter table | 14H | 07:00 | 60H | 60H |
| | | 15H | 15:08 | 00H | 00H |
| | | 16H | 23:16 | 00H | 00H |
| Unused | Contains 0xFFH and can never be changed | 17H | 31:24 | FFH | FFH |

Table 4. Parameter Table (0): JEDEC Flash Parameter Tables

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|--|------------------|-----------------|-----------|------|
| Block/Sector Erase Size | 00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase | 30H | 01:00 | 01b | E5H |
| Write Granularity | 0: 1Byte, 1: 64Byte or larger | | 02 | 1b | |
| Write Enable Instruction Requested for Writing to Volatile Status Registers | 0: Nonvolatile status bit 1: Volatile statusbit (BP status register bit) | | 03 | 0b | |
| Write Enable Opcode Select for Writing to Volatile Status Registers | 0: Use 50H Opcode, 1: Use 06H Opcode, Note:If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b. | | 04 | 0b | |
| Unused | Contains 111b and can never be changed | | 07:05 | 111b | |
| 4KB Erase Opcode | | 31H | 15:08 | 20H | 20H |
| (1-1-2) Fast Read | 0=Not support, 1=Support | 32H | 16 | 1b | F1H |
| Address Bytes Number used in addressing flash array | 00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved | | 18:17 | 00b | |
| Double Transfer Rate (DTR) clocking | 0=Not support, 1=Support | | 19 | 0b | |
| (1-2-2) Fast Read | 0=Not support, 1=Support | | 20 | 1b | |
| (1-4-4) Fast Read | 0=Not support, 1=Support | | 21 | 1b | |
| (1-1-4) Fast Read | 0=Not support, 1=Support | | 22 | 1b | |
| Unused | | | 23 | 1b | |
| Unused | | 33H | 31:24 | FFH | FFH |
| Flash Memory Density | | 37H:34H | 31:00 | 007FFFFFH | |
| (1-4-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 38H | 04:00 | 00100b | 44H |
| (1-4-4) Fast Read Number of Mode Bits | 000b:Mode Bits not support | | 07:05 | 010b | |
| (1-4-4) Fast Read Opcode | | 39H | 15:08 | EBH | EBH |
| (1-1-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3AH | 20:16 | 01000b | 08H |
| (1-1-4) Fast Read Number of Mode Bits | 000b:Mode Bits not support | | 23:21 | 000b | |
| (1-1-4) Fast Read Opcode | | 3BH | 31:24 | 6BH | 6BH |

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|---|------------------|-----------------|--------|-------|
| (1-1-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3CH | 04:00 | 01000b | 08H |
| (1-1-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 07:05 | 000b | |
| (1-1-2) Fast Read Opcode | | 3DH | 15:08 | 3BH | 3BH |
| (1-2-2) Fast Read Number of Wait states | | 3EH | 20:16 | 00010b | 42H |
| (1-2-2) Fast Read Number of Mode Bits | | | 23:21 | 010b | |
| (1-2-2) Fast Read Opcode | | 3FH | 31:24 | BBH | BBH |
| (2-2-2) Fast Read | 0=not support 1=support | 40H | 00 | 0b | EEH |
| Unused | | | 03:01 | 111b | |
| (4-4-4) Fast Read | 0=not support 1=support | | 04 | 1b | |
| Unused | | | 07:05 | 111b | |
| Unused | | 43H:41H | 31:08 | 0xFFH | 0xFFH |
| Unused | | 45H:44H | 15:00 | 0xFFH | 0xFFH |
| (2-2-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 46H | 20:16 | 00000b | 00H |
| (2-2-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (2-2-2) Fast Read Opcode | | 47H | 31:24 | FFH | FFH |
| Unused | | 49H:48H | 15:00 | 0xFFH | 0xFFH |
| (4-4-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 4AH | 20:16 | 00000b | 00H |
| (4-4-4) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (4-4-4) Fast Read Opcode | | 4BH | 31:24 | FFH | FFH |
| Sector Type 1 Size | Sector/block size=2 ^N bytes 0x00b: this sector type don't exist | 4CH | 07:00 | 0CH | 0CH |
| Sector Type 1 erase Opcode | | 4DH | 15:08 | 20H | 20H |
| Sector Type 2 Size | Sector/block size=2 ^N bytes 0x00b: this sector type don't exist | 4EH | 23:16 | 0FH | 0FH |
| Sector Type 2 erase Opcode | | 4FH | 31:24 | 52H | 52H |
| Sector Type 3 Size | Sector/block size=2 ^N bytes 0x00b: this sector type don't exist | 50H | 07:00 | 10H | 10H |
| Sector Type 3 erase Opcode | | 51H | 15:08 | D8H | D8H |

| | | | | | |
|----------------------------|---|-----|-------|-----|-----|
| Sector Type 4 Size | Sector/block size=2 ^N bytes 0x00b: this sector type don't exist | 52H | 23:16 | 00H | 00H |
| Sector Type 4 erase Opcode | | 53H | 31:24 | FFH | FFH |

Table 5. Parameter Table (1): XTX Flash Parameter Tables

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|--|---|------------------|-----------------|-------|-------|
| Vcc Supply Maximum Voltage | 2000H=2.000V 2700H=2.700V 3600H=3.600V | 61H:60H | 15:00 | 3600H | 3600H |
| Vcc Supply Minimum Voltage | 1650H=1.650V 2250H=2.250V 2300H=2.300V 2700H=2.700V | 63H:62H | 31:16 | 2700H | 2700H |
| HW Reset# pin | 0=not support 1=support | 65H:64H | 00 | 0b | 7994H |
| HW Hold# pin | 0=not support 1=support | | 01 | 1b | |
| Deep Power Down Mode | 0=not support 1=support | | 02 | 1b | |
| SW Reset | 0=not support 1=support | | 03 | 1b | |
| SW Reset Opcode | Should be issue Reset Enable(66H) before Reset cmd | | 11:04 | 99H | |
| Program Suspend/Resume | 0=not support 1=support | | 12 | 0b | |
| Erase Suspend/Resume | 0=not support 1=support | | 13 | 0b | |
| Unused | | | 14 | 1b | |
| Wrap-Around Read mode | 0=not support 1=support | | 15 | 1b | |
| Wrap-Around Read mode Opcode | | 66H | 23:16 | FFH | FFH |
| Wrap-Around Read data length | 08H:support 8B wrap-around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B | 67H | 31:24 | 64H | 64H |
| Individual block lock | 0=not support 1=support | 6BH:68H | 00 | 0b | E3FCH |
| Individual block lock bit (Volatile/Nonvolatile) | 0=Volatile 1=Nonvolatile | | 01 | 0b | |
| Individual block lock Opcode | | | 09:02 | FFH | |
| Individual block lock Volatile protect bit default protect status | 0=protect 1=unprotect | | 10 | 0b | |
| Secured OTP | 0=not support 1=support | | 11 | 0b | |
| Read Lock | 0=not support 1=support | | 12 | 0b | |
| Permanent Lock | 0=not support 1=support | | 13 | 1b | |
| Unused | | | 15:14 | 11b | |
| Unused | | | 31:16 | FFFFH | FFFFH |

1.7. ELECTRICAL CHARACTERISTICS

1.7.1 Power-on Timing

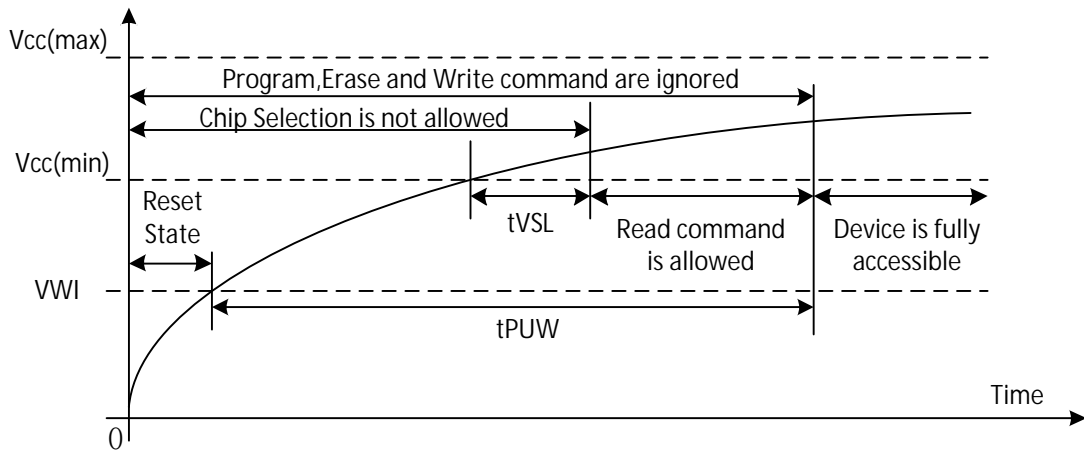


Table3. Power-Up Timing and Write Inhibit Threshold

Note: At power-down, need to ensure VCC drop to 0.5V before the next power-on in order for the device to have a proper power-on reset.

| Symbol | Parameter | Min | Max | Unit |
|-----------|-------------------------------------|-----|-----|------|
| t_{VSL} | VCC(min) To CS# Low | 10 | | us |
| t_{PUW} | Time Delay Before Write Instruction | 1 | - | ms |
| V_{WI} | Write Inhibit Voltage | 1.5 | 2.5 | V |

1.7.2 Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFH). The Status Register contains 00H (all Status Register bits are 0).

1.7.3 Data Retention and Endurance

| Parameter | Typical | Unit |
|-----------------------------|---------|--------|
| Pattern Data Retention Time | 20 | Years |
| Erase/Program Endurance | 100K | Cycles |

1.7.4 Latch up Characteristics

| Parameter | Min | Max |
|--|--------|----------|
| Input Voltage Respect To VSS On I/O Pins | -1.0V | VCC+1.0V |
| VCC Current | -100mA | 100mA |

1.7.5 Absolute Maximum Ratings

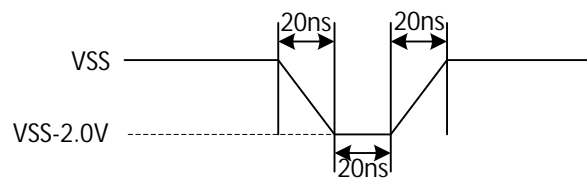
| Parameter | Value | Unit |
|-------------------------------|-------------|------|
| Ambient Operating Temperature | -40 to 85 | °C |
| Storage Temperature | -65 to 150 | °C |
| Output Short Circuit Current | 200 | mA |
| Applied Input/Output Voltage | -0.5 to 4.0 | V |
| VCC | -0.5 to 4.0 | V |

1.7.6 Capacitance Measurement Condition

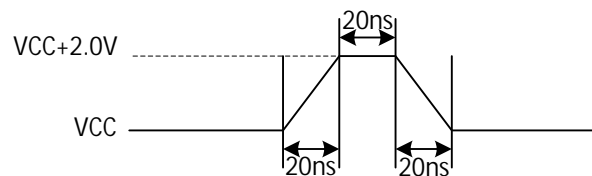
| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|--------|---------------------------------|------------------|--------|-----|------|------------|
| CIN | Input Capacitance | | | 6 | pF | VIN=0V |
| COUT | Output Capacitance | | | 8 | pF | VOU=0V |
| CL | Load Capacitance | | 30 | | pF | |
| | Input Rise And Fall time | | | 5 | ns | |
| | Input Pulse Voltage | 0.1VCC to 0.8VCC | | | V | |
| | Input Timing Reference Voltage | 0.2VCC to 0.7VCC | | | V | |
| | Output Timing Reference Voltage | | 0.5VCC | | V | |

Figure36. Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



1.7.7 DC Characteristics

(T=-40°C~85°C,VCC=2.70~3.60V)

| Symbol | Parameter | Test Condition | Min. | Typ | Max. | Unit |
|-----------------|--|---|---------|-----|---------|------|
| I _{LI} | Input Leakage Current ⁽¹⁾ | | | | ±2 | μA |
| I _{LO} | Output Leakage Current ⁽¹⁾ | | | | ±2 | μA |
| ICC1 | Standby Current | CS#=VCC VIN=VCC or VSS | | 12 | 40 | μA |
| ICC2 | Deep Power-Down Current | CS#=VCC VIN=VCC or VSS | | 0.1 | 4 | μA |
| ICC3 | Operating Current(Read) ⁽²⁾ | CLK=0.1VCC/0.9VCC at 108MHz, Q=Open(*1,*2,*4 I/O) | | 15 | 20 | mA |
| | | CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O) | | 13 | 18 | mA |
| | | CLK=0.1VCC/0.9VCC at 50MHZ,Q=Open(*1,*2,*4) | | 7 | 10 | mA |
| ICC4 | Operating Current(PP) | CS#=VCC | | | 30 | mA |
| ICC5 | Operating Current(WRSR) | CS#=VCC | | | 30 | mA |
| ICC6 | Operating Current(SE) | CS#=VCC | | | 30 | mA |
| ICC7 | Operating Current(BE) | CS#=VCC | | | 30 | mA |
| V _{IL} | Input Low Voltage | | -0.5 | | 0.2VCC | V |
| V _{IH} | Input High Voltage | | 0.7VCC | | VCC+0.4 | V |
| V _{OL} | Output Low Voltage | IOL=1.6mA | | | 0.4 | V |
| V _{OH} | Output High Voltage | IOH=-100uA | VCC-0.2 | | | V |

Notes:

1. Tested on sample basis and specified through design and characterization data, T= 25° C.
2. Pattern 00 or FF. Typical values given for T=25°C. Value guaranteed by design and/or characterization, not 100% tested in production.



1.7.8 AC Characteristics ($T=-40^{\circ}\text{C}\sim 85^{\circ}\text{C}$, $V_{CC}=2.70\sim 3.60\text{V}$, $C_L=30\text{pF}$)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|--|--------|------|------|---------------|
| fC | Serial Clock Frequency For: Fast Read (0BH), Dual Output(3BH), Dual I/O (BBH) | | | 108 | MHz |
| fC1 | Serial Clock Frequency For: Quad I/O(EBH), Quad Output(6BH) | | | 86 | MHz |
| fC2 | Serial Clock Frequency For QPI (0BH, EBH) | | | 72 | MHz |
| fR | Serial Clock Frequency For: Read Data(03H), Read Identification ID(9FH), Read Manufacture ID (90H) | | | 72 | MHz |
| tCLH | Serial Clock High Time | 45% PC | | | ns |
| tCLL | Serial Clock Low Time | 45% PC | | | ns |
| tCLCH | Serial Clock Rise Time(Slew Rate) | 0.2 | | | V/ns |
| tCHCL | Serial Clock Fall Time(Slew Rate) | 0.2 | | | V/ns |
| tSLCH | CS# Active Setup Time | 5 | | | ns |
| tCHSH | CS# Active Hold Time | 5 | | | ns |
| tSHCH | CS# Not Active Setup Time | 5 | | | ns |
| tCHSL | CS# Not Active Hold Time | 5 | | | ns |
| tSHSL | CS# High Time (read/write) | 20 | | | ns |
| tSHOZ | Output Disable Time | | | 9 | ns |
| tCLOX | Output Hold Time | 1 | | | ns |
| tDVCH | Data In Setup Time | 2 | | | ns |
| tCHDX | Data In Hold Time | 2 | | | ns |
| tHLCH | Hold# Low Setup Time(relative to Clock) | 5 | | | ns |
| tHHCH | Hold# High Setup Time(relative to Clock) | 5 | | | ns |
| tCHHL | Hold# High Hold Time(relative to Clock) | 5 | | | ns |
| tCHHH | Hold# Low Hold Time(relative to Clock) | 5 | | | ns |
| tCLOV | Clock Low To Output Valid | | | 7.5 | ns |
| tWHSL | Write Protect Setup Time Before CS# Low | 20 | | | ns |
| tSHWL | Write Protect Hold Time After CS# High | 100 | | | ns |
| tDP | CS# High To Deep Power-Down Mode | | | 0.1 | μs |
| tRES1 | CS# High To Standby Mode Without Electronic Signature Read | | | 20 | μs |
| tRES2 | CS# High To Standby Mode With Electronic Signature Read | | | 20 | μs |
| tRST_R | CS# High To Next Command After Reset (from read) | | | 20 | μs |
| tRST_P | CS# High To Next Command After Reset (from program) | | | 20 | μs |
| tRST_E | CS# High To Next Command After Reset (from erase) | | | 12 | ms |
| tW | Write Status Register Cycle Time | | 60 | 5000 | ms |
| tPP | Page Programming Time | | 0.3 | 0.7 | ms |
| tSE | Sector Erase Time | | 60 | 5000 | ms |
| tBE ₁ | Block Erase Time(32K Bytes) | | 0.15 | 1.2s | s |
| tBE ₂ | Block Erase Time(64K Bytes) | | 0.25 | 1.6s | s |
| tCE | Chip Erase Time | | 22 | 60 | s |

Note:

1. Clock high or Clock low must be more than or equal to 45%Pc. $P_c = 1/f_c(\text{MAX})$
2. Maximum Serial Clock Frequencies are measured results picked at the falling edge.
3. Typical values given for $T_A = 25^\circ\text{C}$. Value guaranteed by design and/or characterization, are not 100% tested in production.

Figure 39. Serial Input Timing

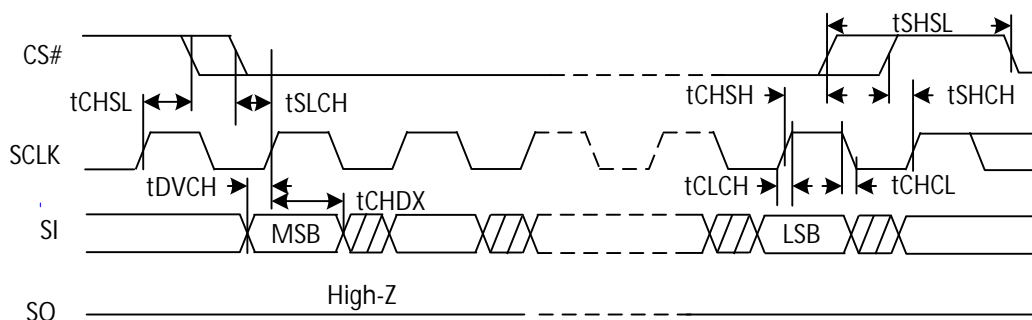


Figure 40. Output Timing

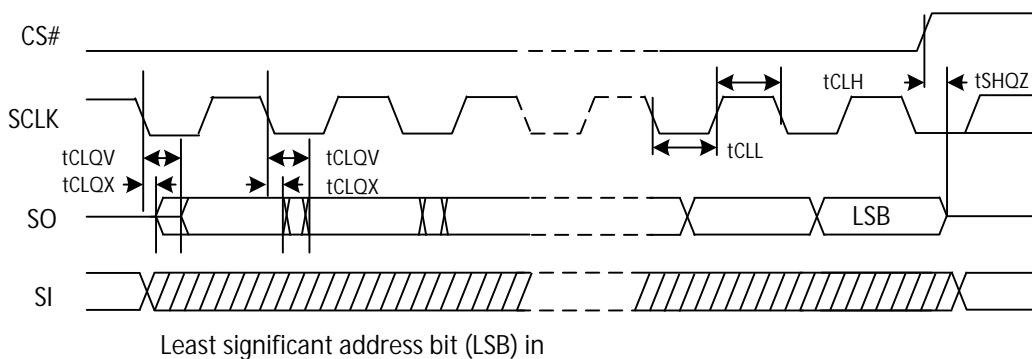
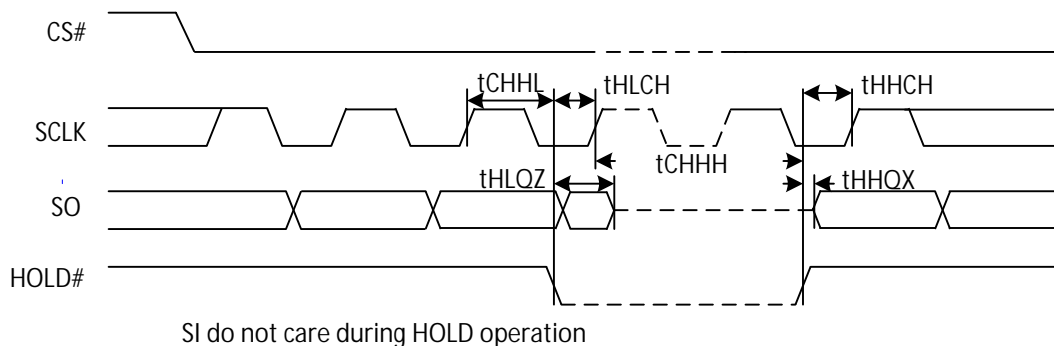


Figure 41. Hold Timing



QPI_PSRAM

GENERAL DESCRIPTION

This Pseudo-SRAM device features a high speed, low pin count interface. It has 4 SDR I/O pins and operates in SPI (serial peripheral interface) or QPI (quad peripheral interface) mode with frequencies up to 109MHz. The data input (A/DQ) to the memory relies on clock (CLK) to latch all instructions, addresses and data. It is most suitable for low-power and low cost portable applications. It incorporates a seamless self-managed refresh mechanism. Hence it does not require the support of DRAM refresh from system host. The self-refresh feature is a special design to maximize performance of memory read operation.

Signal Table

All signals are listed in Table 2.

Table 2: Signals Table

| Symbol | Type | SPI Mode Function | QPI Mode Function | Comments |
|------------------|--------|---|-------------------|----------|
| VDD | Power | Core supply 3.3V | | |
| VSS | Ground | Core supply ground | | |
| CE# | Input | Chip select, active low. When CE#=1, chip is in standby state | | |
| CLK | Input | Clock Signal | | |
| SI/SIO[0] | IO | Serial Input | IO[0] | |
| SO/SIO[1] | IO | Serial Output | IO[1] | |
| SIO[2] | IO | -- | IO[2] | |
| SIO[3] | IO | -- | IO[3] | |

Power-Up Initialization

SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When VDD reaches a stable level at or above minimum VDD, the device will require 150μs and user-issued RESET Operation (see section 12) to complete its self-initialization process. From the beginning of power ramp to the end of the 150μs period, CLK should remain LOW, CE# should remain HIGH (track VDD within 200mV) and SI/SO/SIO [3:0] should remain LOW.

After the 150μs period the device is ready for normal operation.

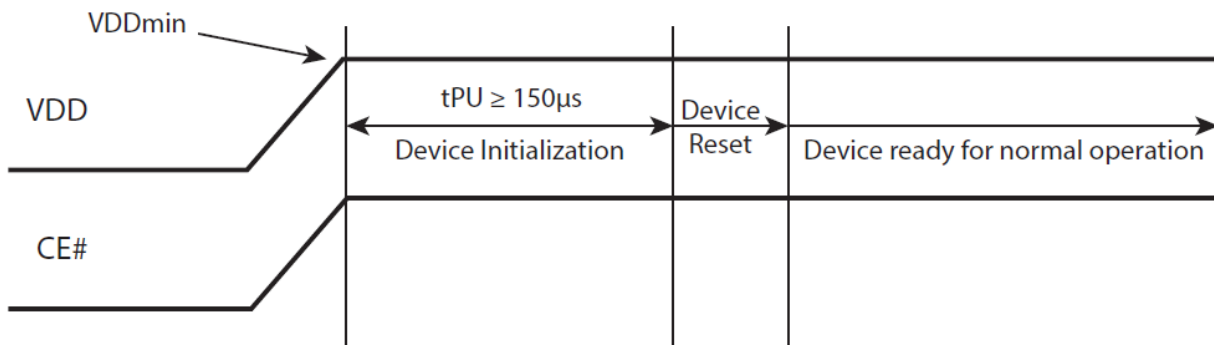


Figure 1. Power-Up Initialization Timing

Interface Description

2.1.1. Address Space

SPI/QPI PSRAM device is byte - addressable. 64M device is addressed with A[22:0].

2.1.2. Page Size

Page size is 1K (CA[9:0]). Default burst setting is Linear Bursting that crosses page boundary in a continuous manner. Note however that burst operations which can cross page boundary have a lower max input clock frequency of 84MHz. Optionally the device can also be set to wrap 32 (CA[4:0]) via the Wrap Boundary Toggle command and is not allowed to cross page boundary in this configuration.

2.1.3. Drive Strength

The device powers up in 50Ω.

2.1.4. Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

2.1.5. Command/Address Latching Truth Table

The device recognizes the following commands specified by the various input methods.

| | | SPI Mode | | | | | QPI Mode | | | | |
|---|------|----------|------|------------|-----|-----------|--------------|------|------------|-----|-----------|
| Command | Code | Cmd | Addr | Wait Cycle | DIO | Max Freq. | Cmd | Addr | Wait Cycle | DIO | Max Freq. |
| Read | 'h03 | S | S | 0 | S | 33 | N/A | | | | |
| Fast Read | 'h0B | S | S | 8 | S | 109/84* | Q | Q | 4 | Q | 66 |
| Fast Read Quad | 'hEB | S | Q | 6 | Q | 109/84* | Q | Q | 6 | Q | 109/84* |
| Write | 'h02 | S | S | 0 | S | 109/84* | Q | Q | 0 | Q | 109/84* |
| Quad Write | 'h38 | S | Q | 0 | Q | 109/84* | same as 'h02 | | | | |
| Enter Quad Mode | 'h35 | S | - | - | - | 109 | N/A | | | | |
| Exit Quad Mode | 'hF5 | N/A | | | | | Q | - | - | - | 109 |
| Reset Enable | 'h66 | S | - | - | - | 109 | Q | - | - | - | 109 |
| Reset | 'h99 | S | - | - | - | 109 | Q | - | - | - | 109 |
| Wrap Boundary Toggle | 'hC0 | S | - | - | - | 109 | Q | - | - | - | 109 |
| Read ID | 'h9F | S | S | 0 | S | 109 | N/A | | | | |
| Remark: S = Serial IO, Q = Quad IO | | | | | | | | | | | |
| Note *:Max 109Mhz(PKG VDD= 3.3V+-10%) in Wrap Mode and Max 84Mhz(PKG VDD= 3.3V+-10%) in Linear Burst Mode | | | | | | | | | | | |
| If Max frequency 133Mhz(PKG VDD= 3.0V+-10%) requested, please contact XTX sales and FAE. | | | | | | | | | | | |

2.1.6. Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active command and set the device into standby. Not doing so will block internal refresh operations and cause memory failure.

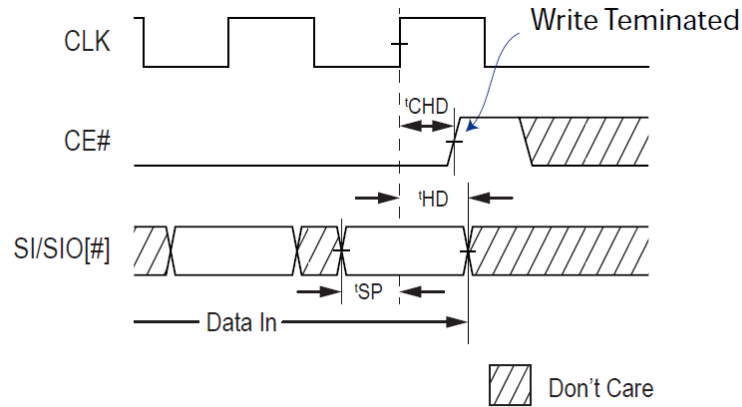


Figure 2: Write Command Termination

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time ($t_{CHD} > t_{ACLK} + t_{CLK}$) for a sufficient data window.

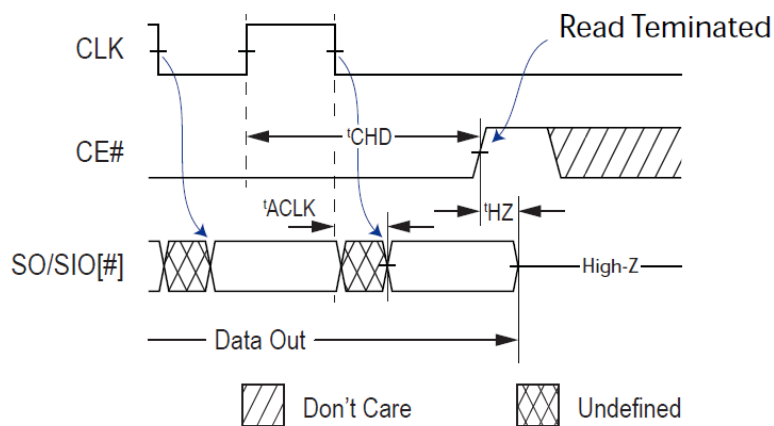


Figure 3: Read Command Termination

Wrap Boundary Toggle Operation

The Wrap Boundary Toggle Operation switches the device's wrapped boundary between Linear Burst which crosses the 1K page boundary (CA[9:0]) and wrap 32 (CA[4:0]) bytes. Default setting is Linear Burst.

Linear Burst allows the device to burst through page boundary. Page boundary crossing is invisible to the memory controller and Linear Burst is limited to a lower max CLK frequency of 84MHz.

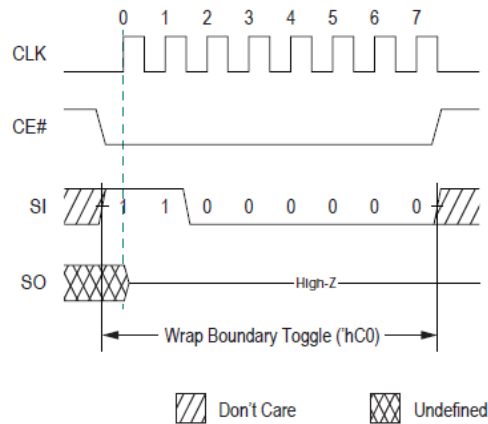


Figure 4: SPI Wrap Boundary Toggle 'hC0

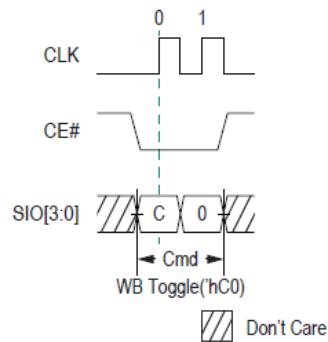


Figure 5: QPI Wrap Boundary Toggle 'hC0

SPI Mode Operations

The device powers up into SPI mode by default but can also be switched into QPI mode.

2.1.7. SPI Read Operations

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

SPI Reads can be done in three ways:

1. 'h03: Serial CMD, Serial IO, slow frequency, with linear or burst wrap of 32 byte configurability.
2. 'h0B: Serial CMD, Serial IO, fast frequency, with burst wrap of 32 byte.
3. 'hEB: Serial CMD, Quad IO, fast frequency, with burst wrap of 32 byte.

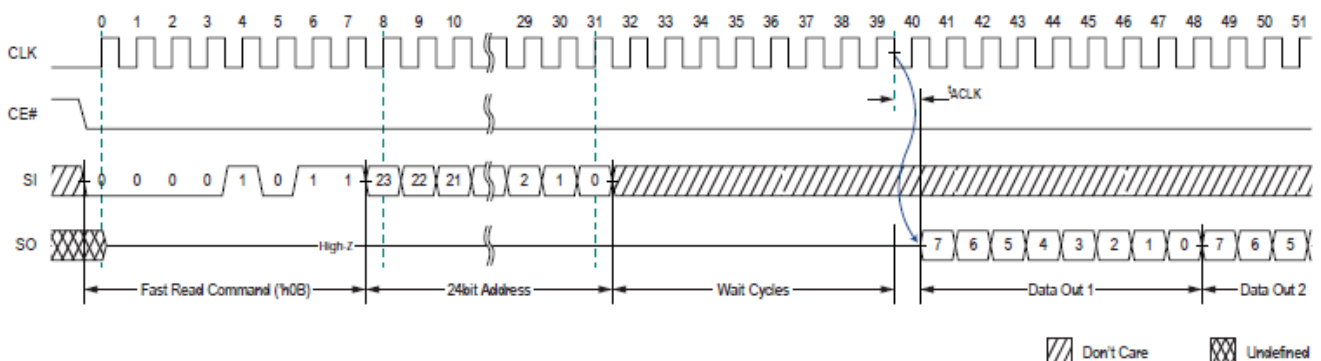
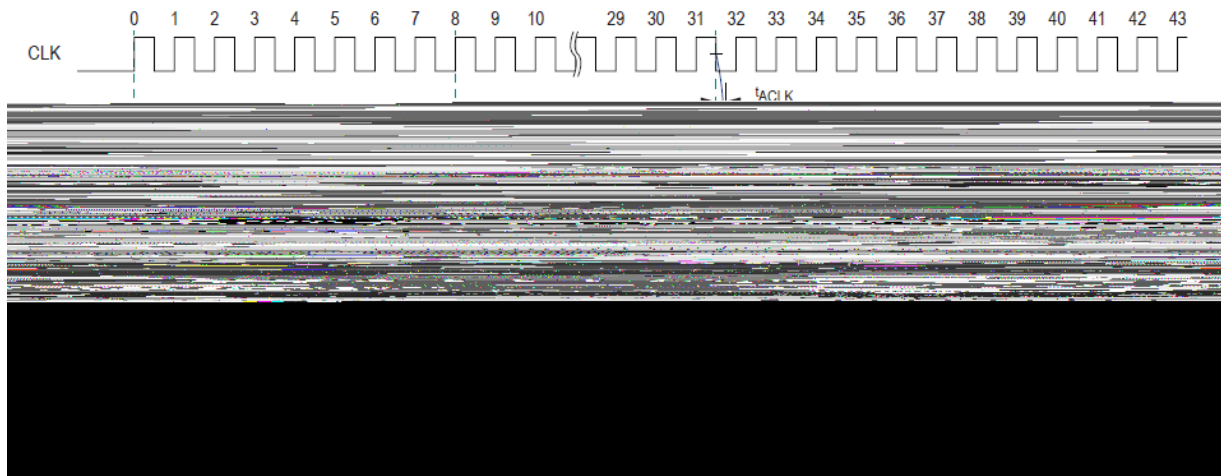


Figure 7: SPI Fast Read 'h0B (max freq 133 MHz)

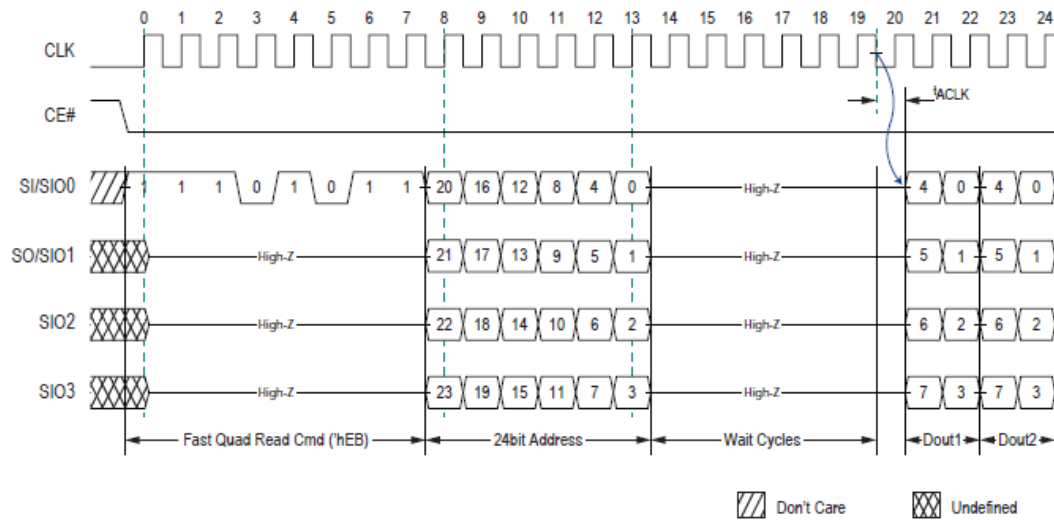


Figure 8: SPI Fast Quad Read 'hEB (max freq 133 MHz)

2.1.8. SPI Write Operations

SPI write command can be input as 'h02 or 'h38.

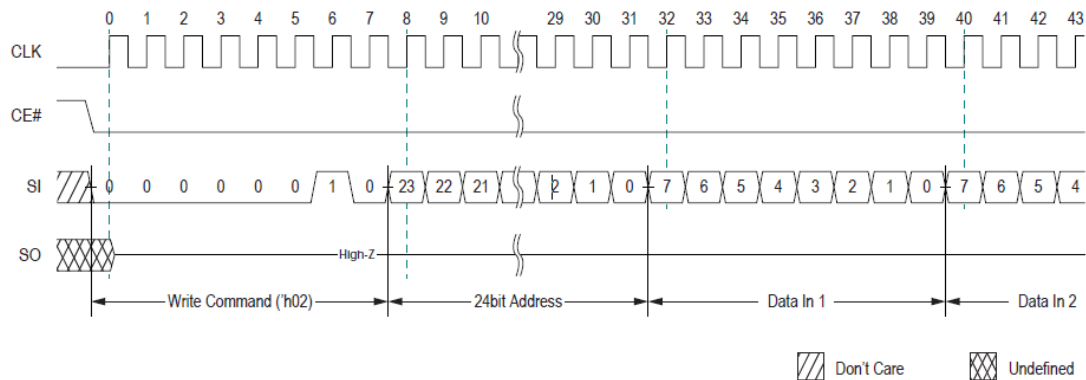


Figure 9: SPI Write 'h02

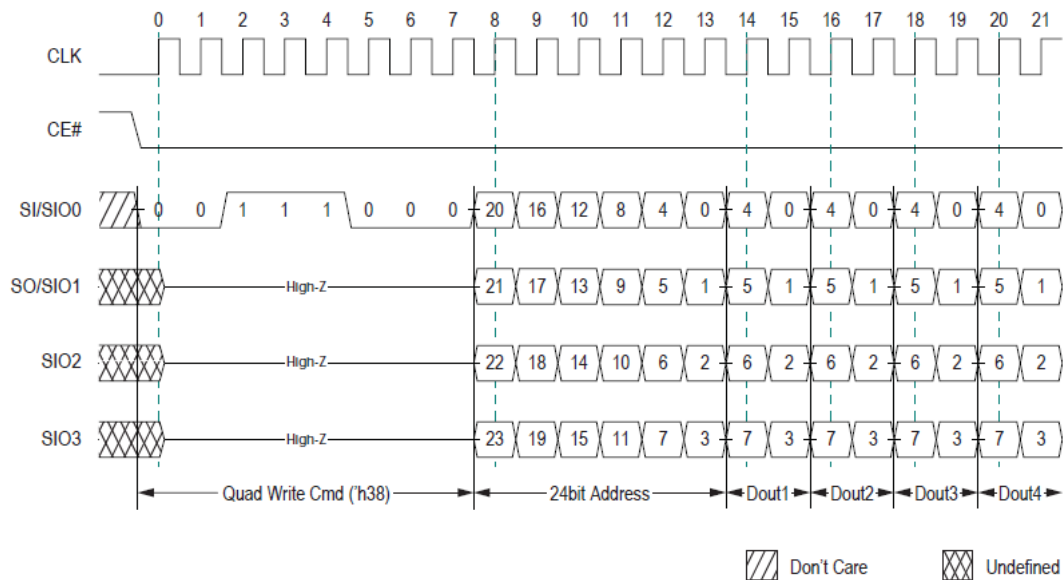


Figure 10: SPI Quad Write 'h38

2.1.9. SPI Quad Mode Enable Operation

This command switches the device into quad IO mode.

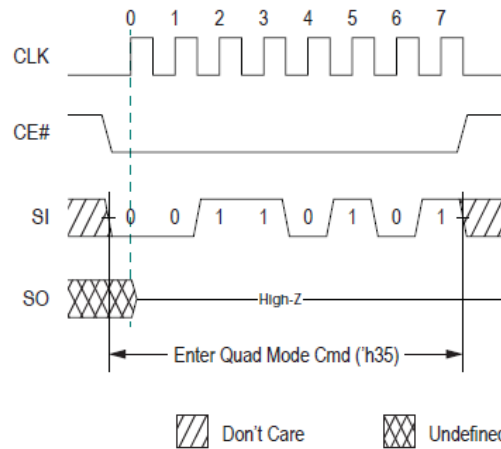


Figure 11: Quad Mode Enable 'h35 (available only in SPI mode)

2.1.10. SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

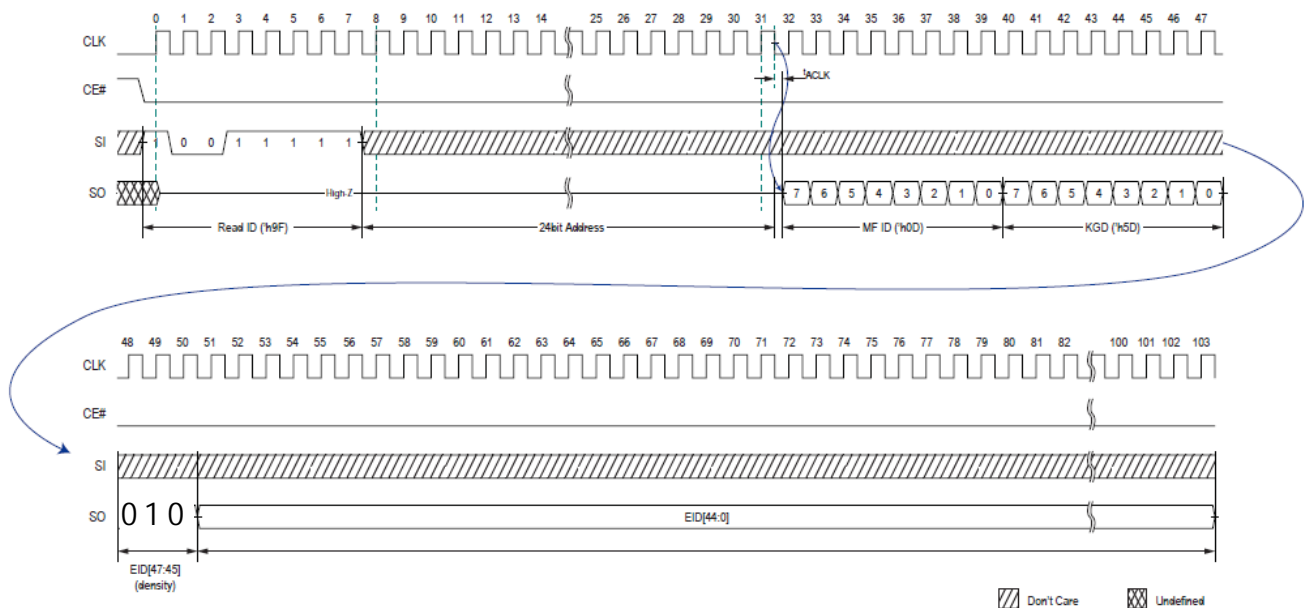


Figure 12: SPI Read ID 'h9F (available only in SPI mode)

Table 3: Known Good Die (KGD)

| KGD[7:0] | Known Good Die |
|-------------|----------------|
| 'b0101_0101 | FAIL |
| 'b0101_1101 | PASS |

*Note: Default is FAIL die, and only mark PASS after all tests passed.

QPI Mode Operations

2.1.11. QPI Read Operation

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

QPI Reads can be done in one of two ways:

1. 'h0B: Quad CMD, Quad IO, slow frequency
2. 'hEB: Quad CMD, Quad IO, fast frequency

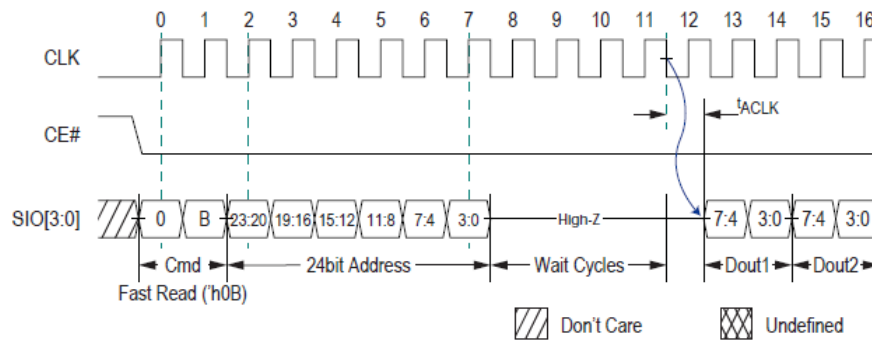


Figure 13: QPI Fast Read 'h0B (max freq 66 MHz)

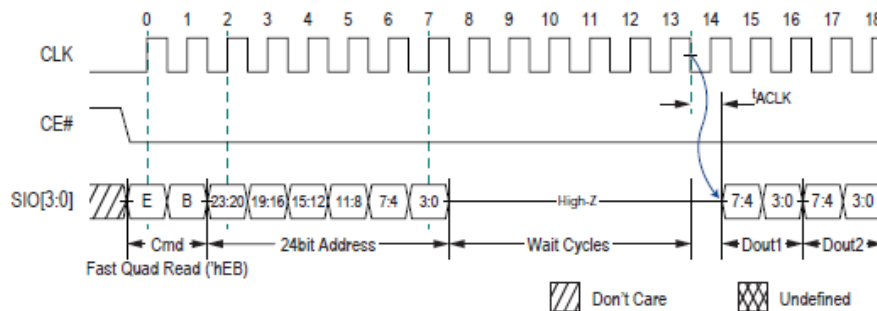


Figure 14: QPI Fast Quad Read 'hEB (max freq 133 MHz)

2.1.12. QPI Write Operation(s)

QPI write command can be input as 'h02 or 'h38.

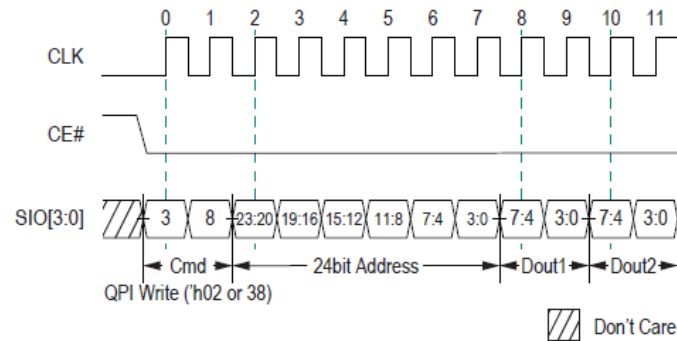


Figure 15: QPI Write 'h02 or 'h38

2.1.13. QPI Quad Mode Exit operation

This command will switch the device back into serial IO mode.

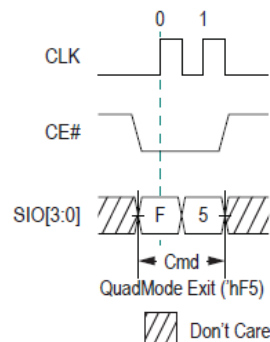


Figure 16: Quad Mode Exit 'hF5 (only available in QPI mode)

Reset Operation

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power - up. This operation consists of two commands: Reset - Enable (RSTEN) and Reset (RST).

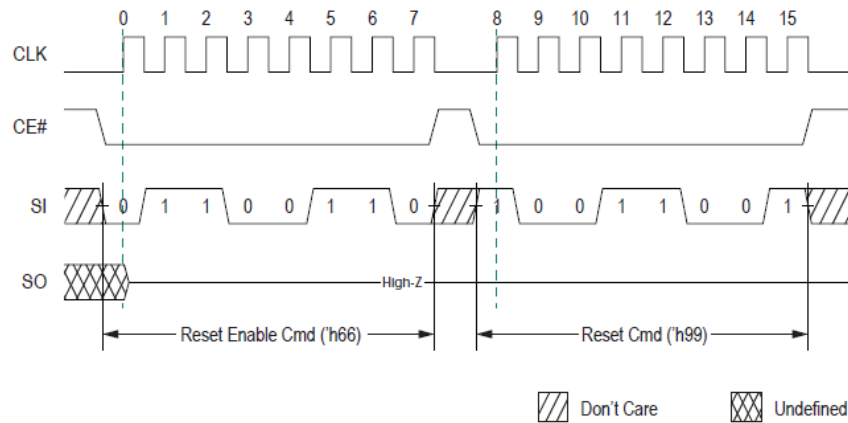


Figure 17: SPI Reset

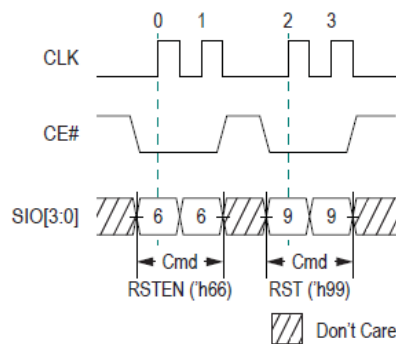


Figure 18: QPI Reset

Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

Input/ Output Timing

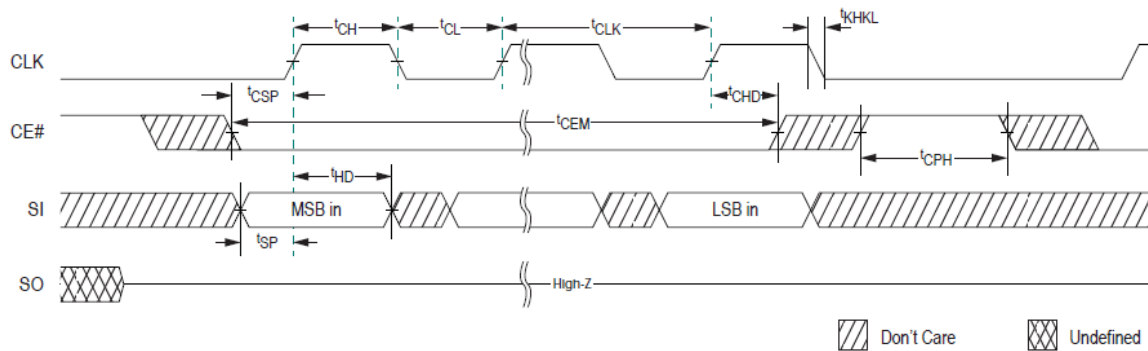


Figure 19: Input Timing

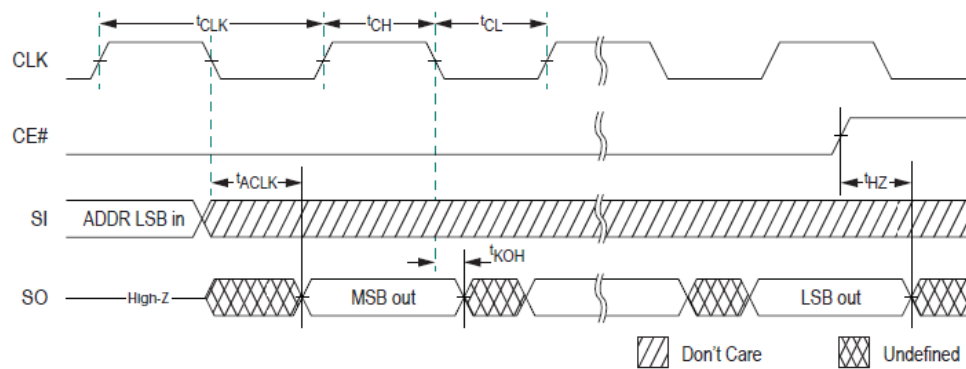


Figure 20: Output Timing

Electrical Specifications

2.1.14. Absolute Maximum Ratings

Table4: Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit | Notes |
|--|--------|-----------------|------|-------|
| Voltage to any ball except VDD relative to VSS | VT | -0.4 to VDD+0.4 | V | |
| Voltage on VDD supply relative to VSS | VDD | -0.4 to +4.0 | V | 2 |
| Storage Temperature | TSTG | -55 to +150 | °C | 1 |

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Notes 2: During voltage transitions, all pins may overshoot to -0.5V or VCC+0.5V for period up to 20ns.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2.1.15. Pin Capacitance

Table 5: Package Pin Capacitance

| Parameter | Symbol | Min | Max | Unit | Notes |
|------------------------|--------|-----|-----|------|---------|
| Input Pin Capacitance | CIN | | 6 | pF | VIN=0V |
| Output Pin Capacitance | COUT | | 8 | pF | VOUT=0V |

Note1: spec'd at 25°C.

Table 6: Load Capacitance

| Parameter | Symbol | Min | Max | Unit | Notes |
|------------------|--------|-----|-----|------|-------|
| Load Capacitance | CL | | 20 | pF | |

Note1: System CL for the use of package

2.1.16. Operating Conditions

Table 8: Operating Characteristics

| Parameter | Min | Max | Unit | Notes |
|----------------------------------|----------|-----|------|-------|
| Operating Temperature (extended) | -40 | 105 | °C | 1 |
| Operating Temperature (standard) | -40(-25) | 85 | °C | |

Note1: spec'd temp range of -40 to 105°C is only characterized; test condition will be -32 to 105°C.

2.1.17. DC Characteristics

Table 9: DC Characteristics

| Symbol | Parameter | Min | Max | Unit | Notes |
|------------|--------------------------------------|---------|---------|------|-------|
| VDD | Supply Voltage | 2.7 | 3.6 | V | |
| VIH | Input high voltage | VDD-0.4 | VDD+0.3 | V | |
| VIL | Input low voltage | -0.3 | 0.4 | V | |
| VOH | Output high voltage (IOH=-0.2mA) | 0.8 VDD | | V | |
| VOL | Output low voltage (IOL=+0.2mA) | | 0.2 VDD | V | |
| ILI | Input leakage current | | 1 | μA | |
| ILO | Output leakage current | | 1 | μA | |
| ICC | Read/Write | | 7 | mA | 1,2 |
| ISBEXT | Standby current (extended temp) | | 350 | μA | 3 |
| ISBSTD | Standby current (standard temp) | | 250 | μA | 3 |
| ISBSTDroom | Standby current (standard room temp) | | 140 | μA | 3,4 |

Note: 1. Output load current not included.

2. Typical Icc 5.5mA at 109Mhz

3. Standby current is measured when CLK is in DC low state.

4. Typical ISB_{STDroom} 100uA

2.1.18. AC Characteristics

Table 10: READ/WRITE Timing

| Symbol | Parameter | Min | Max | Unit | Notes |
|---------|--|------|------|-----------|----------------|
| tCLK | CLK period - SPI Read ('h03) | 30.3 | | | 33MHz |
| | CLK period - QPI Read ('h0B) | 15.1 | | | 66Mhz |
| | CLK period - all other operations | 11.9 | | | 84MHz*1, |
| | CLK period - all other operations PKG 3V | 7.5 | | | 109MHz*1,2,3 |
| | CLK period - all other operations PKG 3.3V | 9.17 | | | 109MHz*2,3 |
| tCH/tCL | Clock high/low width | 0.45 | 0.55 | tCLK(min) | |
| tKHL | CLK rise or fall time | | 1.5 | ns | 3 |
| tCPH | CE# HIGH between subsequent burst operations | 18 | | ns | |
| tCEM | CE# low pulse width | | 4 | μs | Extended grade |
| | | | 8 | | Standard grade |
| tCSP | CE# setup time to CLK rising edge | 2.5 | | ns | |
| tCHD | CE# hold time from CLK rising edge SIP | 2.5 | | ns | 1 |
| | CE# hold time from CLK rising edge PKG | 3.0 | | ns | 2 |
| tSP | Setup time to active CLK edge | 2 | | ns | |
| tHD | Hold time from active CLK edge | 2 | | ns | |
| tHZ | Chip disable to DQ output high-Z | | 5.5 | ns | |
| tACLK | CLK to output delay | 2 | 5.5 | ns | |
| tKOH | Data hold time from clock falling edge | 1.5 | | ns | |
| tRST | Time between end of RST CMD to next val-id CMD | 50 | | ns | |

Note

- 1: Only non-Wrapped type bursts allow page boundary crossing. Frequency limits are therefore 109MHz max without crossing page boundary, and 84MHz max when burst commands cross page boundary
- 2: System max CL 20pF for the use of package. Frequency limits are therefore 109MHz (PKG VDD=3.3V+-10%) max without crossing page boundary, and 84MHz max when burst commands cross page boundary
- 3: For operating frequencies >84MHz, it is highly recommended to utilize CLK falling edge to sample read data or align sampling clock via data pattern tuning (refer to JEDEC JESD84-B50 for an example).
- 4: Measured from 20% to 80% of VDD

**REVISION HISTORY**

| Revision | Description | Date |
|----------|---|--------------|
| 0.1 | Preliminary release | May 30,2020 |
| 0.2 | Revised Max frequency from 133Mhz to 109Mhz | Jul 13, 2020 |